Unconventional Fault-Tolerant Accelerators

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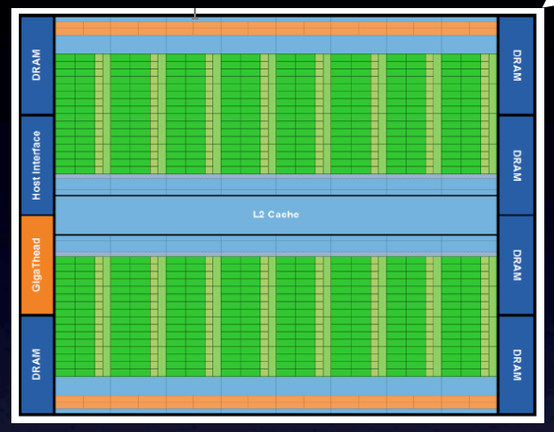
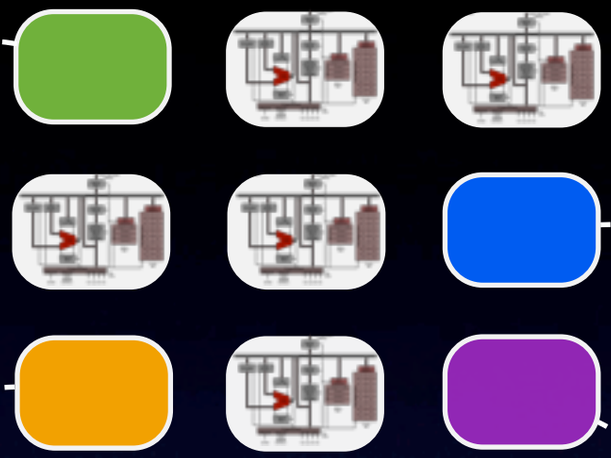
IMS: G. Lecerf, S. Saighi, J. Tomas
and many others...

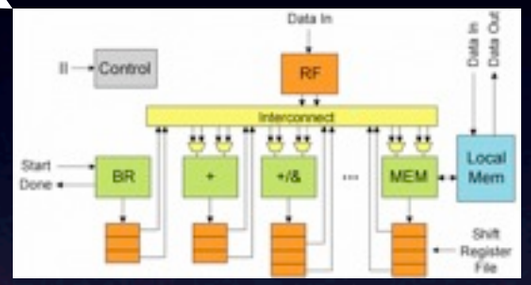
Which Accelerators ?



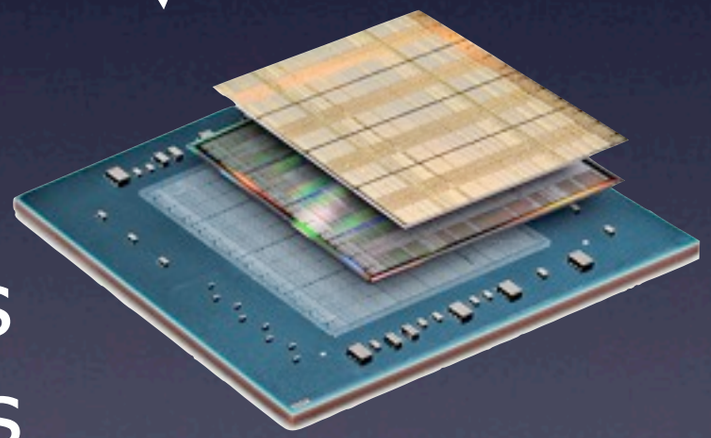
GPUs



Heterogeneous multi-cores



Loop Accelerator (CCCP)



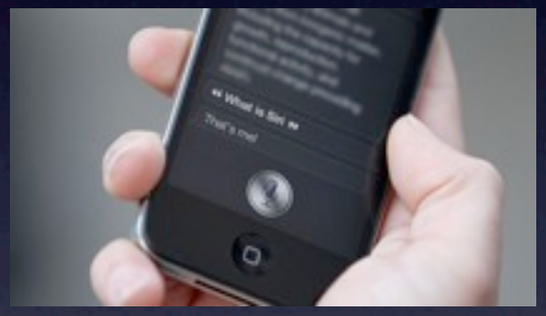
FPGAs
CGRAs

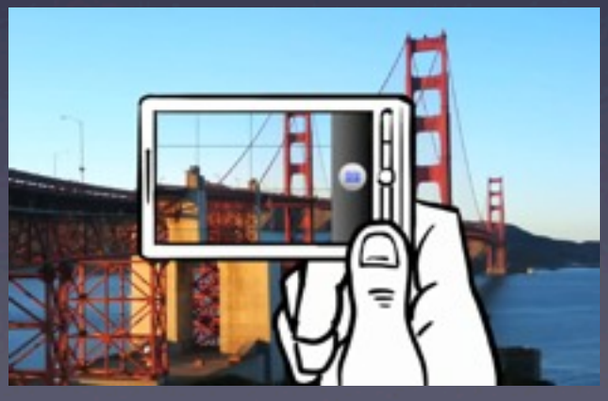
GreenDroid

Multi-Purpose Accelerators

- Performance/Flexibility/Efficiency tradeoff ?

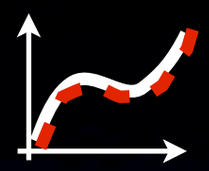
For Which Applications ?

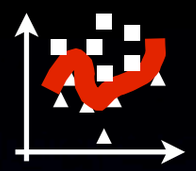




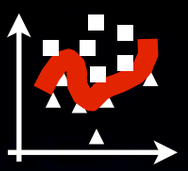
For Which Applications ?

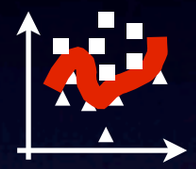
Tolerate inaccuracy


blackschol


bodytrack


canneal

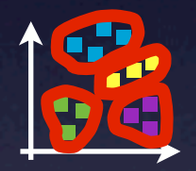

dedup


facesim


ferret

?
fluidanim.


freqmine

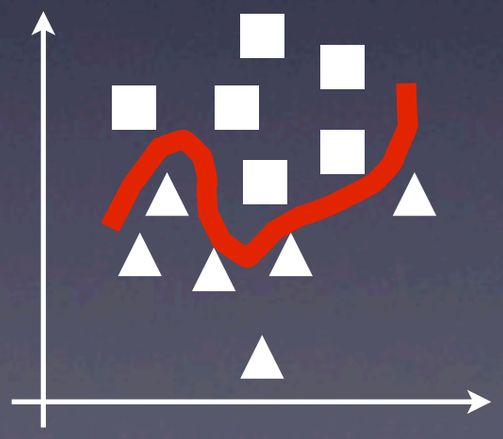

stream cluster

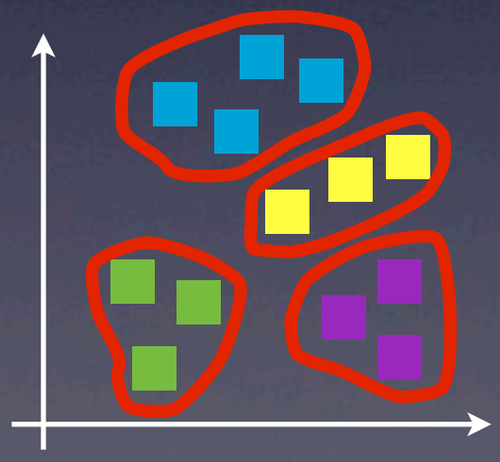

swaptions

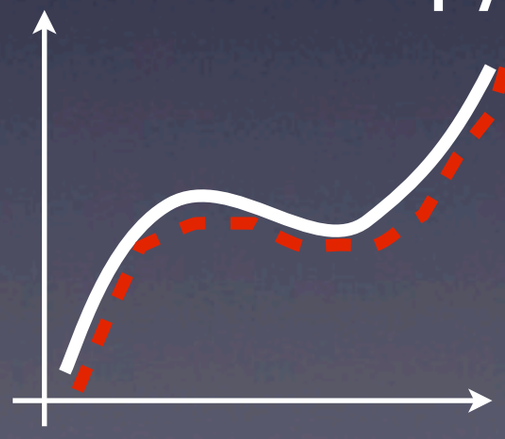

vips

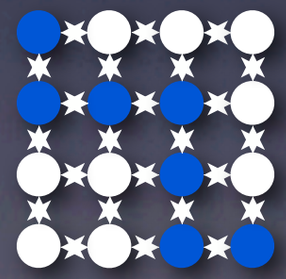
?
x264

PARSEC (RMS)


Classification


Clustering


Approximation

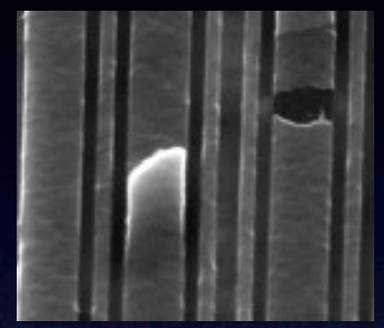

Optimization


Filtering

Inaccuracy-Tolerant Applications

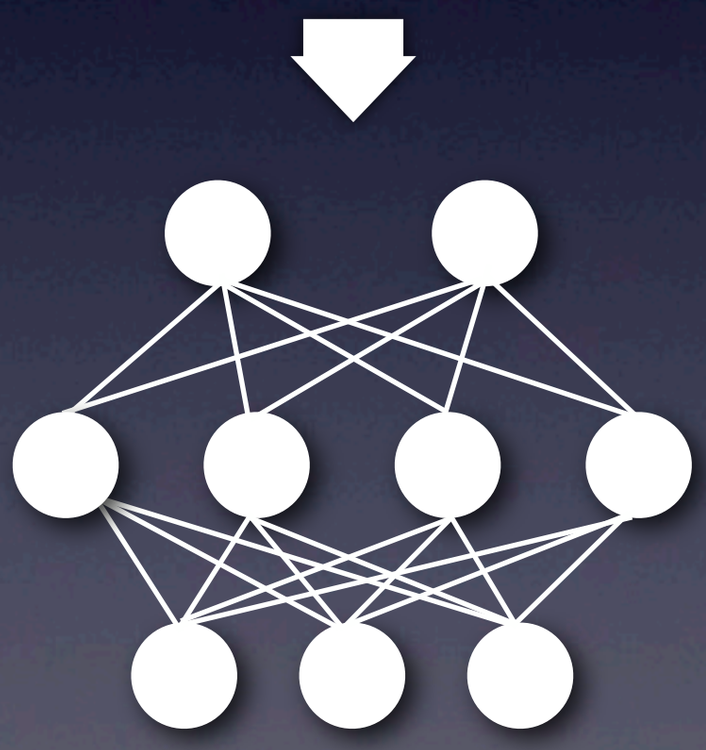
Energy

Defects/ Faults



Intrinsic tolerance to errors

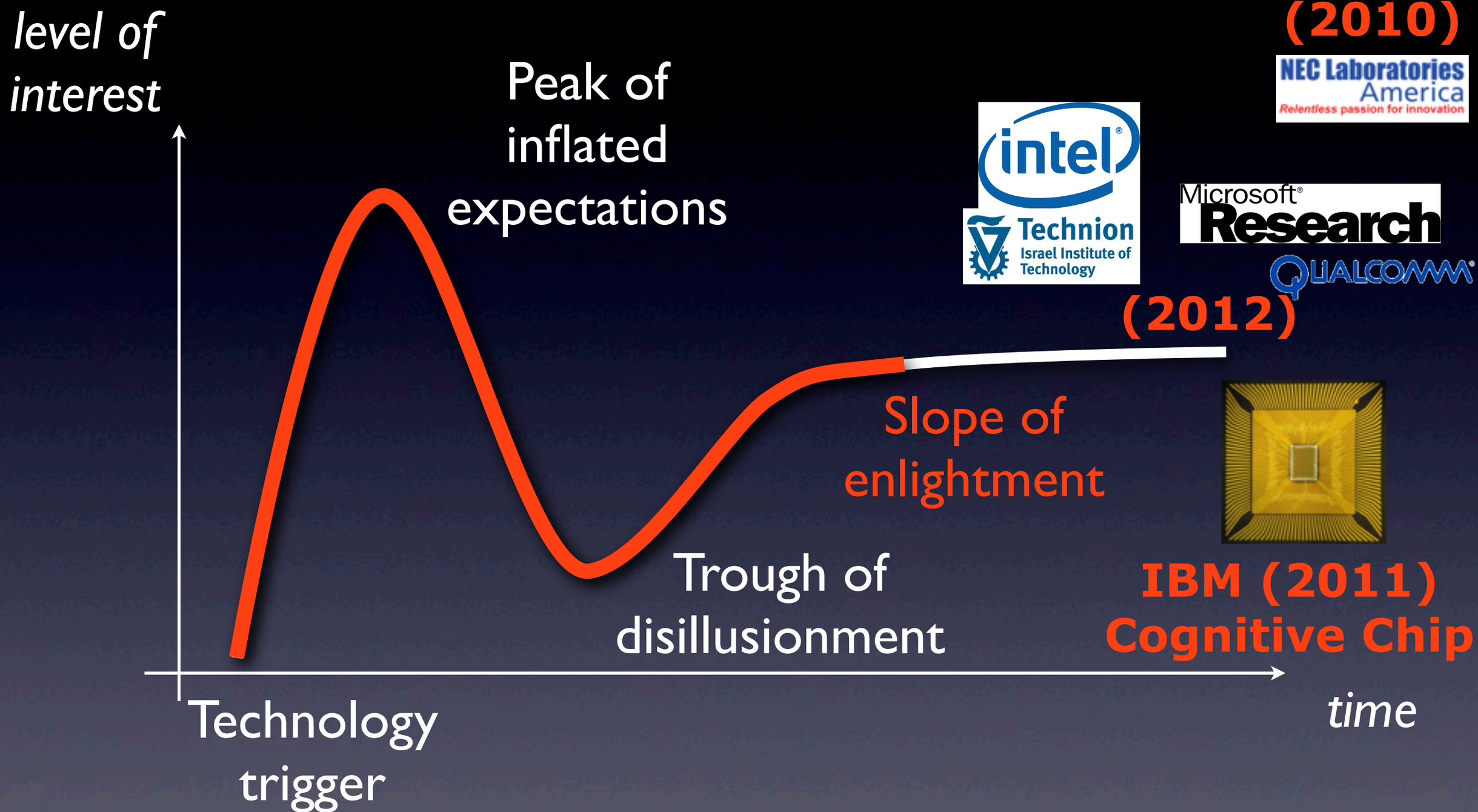
Low energy



Broad potential application scope

Hardware Neural Networks

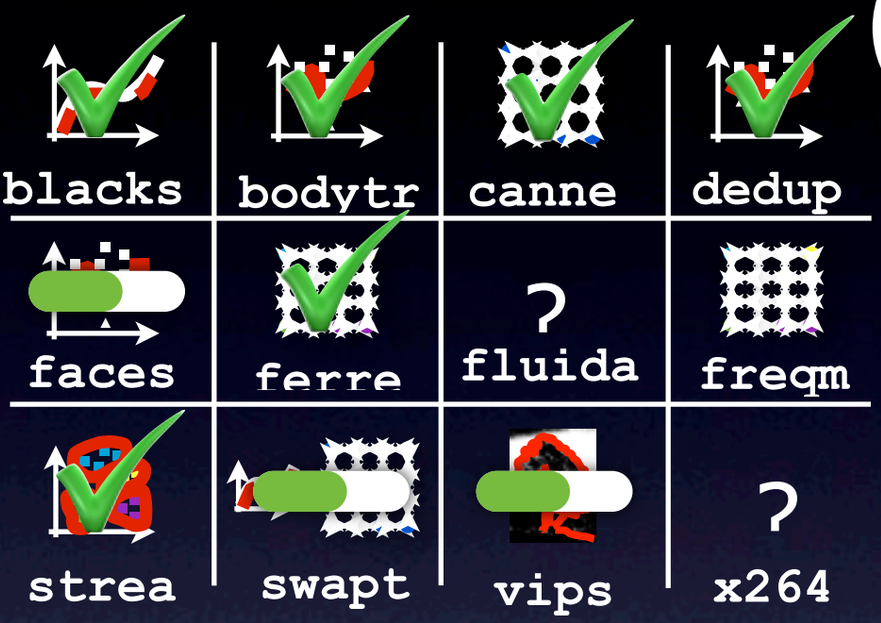
NNs...Again ?!



- New context: ~~Killer micro~~, ~~SVM~~, ~~scientific computing~~

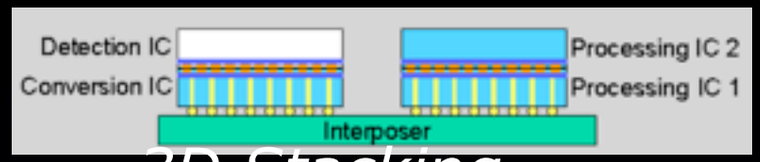
"The Rebirth of NNs", keynote ISCA 2010

Roadmap for NN Adoption



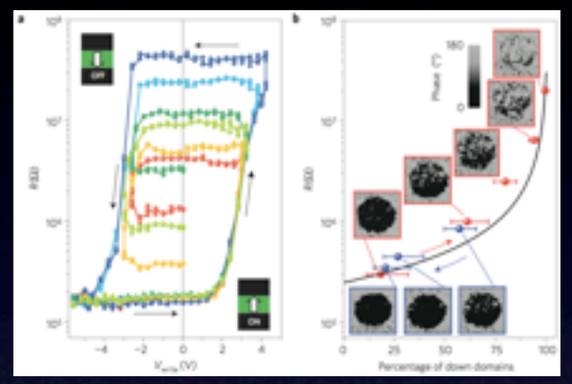
PARSEC using NNs (IISWC 2012)

Application scope ?



3D Stacking (DAC 2012, tape-out: 2013/2014)

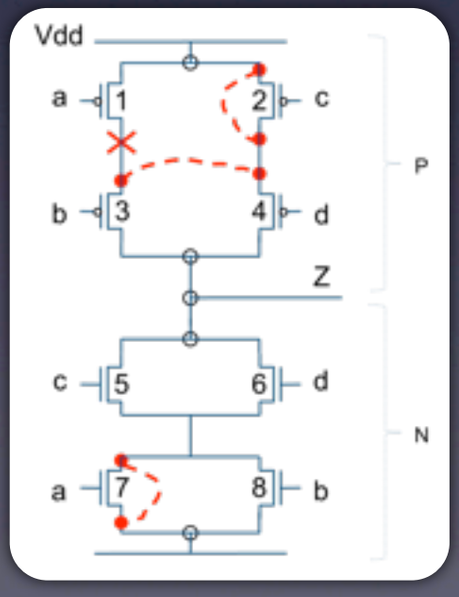
Memristors (tape-out: 2014/2015)



Hardware NNs

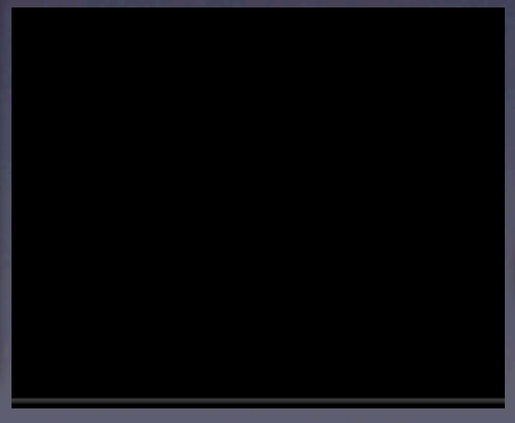
Low Energy ?

Fault Tolerance ?



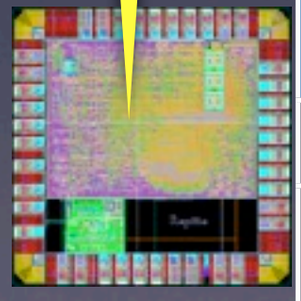
ISCA 2012

Permanent & Transient faults



Tape-Out

2pJ/spike @65nm (IBM: 45pJ/spike @45nm)



90nm	Hardware NN	Intel Stealy (~ Atom at 90nm)
Power	4.70W	2.78W
Energy/ Row	70nJ	68388nJ

Thank You

To advance what we do with computers [...] we need computers that can model events, objects and concepts based on what we show the computers and the data accessible to them.

Pradeep Dubey, "Recognition, Mining and Synthesis moves computers to the era of tera," Technology@Intel Magazine, vol. 9, 2005, pp. 1-10.