THE MULTIPLE-INPUT TRANSLINEAR ELEMENT: A VERSATILE CIRCUIT ELEMENT

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ABSTRACT

We define the multiple-input translinear element (MITE), a versatile circuit primitive from which we can construct low-voltage translinear circuits and log-domain filters. A *K*-input MITE produces an output current that is exponential in a weighted sum of its *K* input voltages. We briefly discuss six MITE implementations and show experimental data from two of these six that we have fabricated in a 2–µm double-poly CMOS process available through MOSIS.

1. TRANSLINEAR CIRCUIT ELEMENTS

In 1975, Barrie Gilbert [1] coined the word *translinear* to describe a class of nonlinear circuits whose operation is based on the exponential current–voltage relationship of the bipolar transistor. The word *translinear* derives from a contraction of one way of expressing the exponential current–voltage relationship of the bipolar—that is, the bipolar's *trans*conductance is *linear* in the current flowing into its collector terminal. The subthreshold MOS transistor also has an exponential current–voltage relationship [2], so we can count it as a translinear device. Notwithstanding some limitations of the subthreshold MOS transistor compared to the bipolar transistor from the standpoint of translinear-circuit implementation [2, 3], the subthreshold MOS transistor has some unique properties that enable us to implement certain translinear circuits with fewer transistors or with lower supply-voltage requirements than we could using bipolar transistors [3–5].

In this paper, we define a new translinear circuit primitive called the *multiple-input translinear element* (MITE). A *K*-input MITE has *K* different *trans*conducances, each of which is *linear* in the MITE's output current. From these elements, we can construct MITE networks [6], a class of translinear network circuits that can embody product-of-power-law relationships in the current signal domain. For a given product-of-power-law relationship, a MITE network implementation will often require fewer transistors and permit a lower power-supply voltage than would a corresponding translinear loop implementation. From MITEs, we can also make log-domain filters [7], a class of filters in the current signal domain that are large-signal linear yet comprise only grounded capacitors, current sources, and translinear (i.e., highly nonlinear) devices.

2. THE MULTIPLE-INPUT TRANSLINEAR ELEMENT

We depict a circuit symbol for an ideal MITE in Fig. 1; the MITE sums *K* input voltages, V_1 through V_K, scaled, respectively, by dimensionless positive coefficients, w_1 through w_K. The MITE then generates a current, *I*, that is exponential in this weighted sum. We assume that we have the ability to control the values of the weighting coefficients proportionally, so we can make accurate ratios of weighting coefficients.

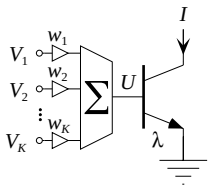

Figure 1. Circuit symbol for an ideal multiple-input translinear element (MITE).

The bipolar transistor shown in Fig. 1 represents an ideal device with an exponential current–voltage characteristic such that the exponential current, *I*, flows into a terminal different from the one to which the controlling voltage, *U*, is applied. This device does not need to be a bipolar transistor, but a diode would not be appropriate in this context. A subthreshold MOS transistor would be a suitable replacement for the bipolar. We can implement the weighted summation operation in a purely passive manner using either a resistive or a capacitive voltage divider. The triangular amplifier symbols, which represent the weighting operation in Fig. 1, convey two different notions. First, they denote that an input voltage, V_k, is scaled by a constant gain whose value is given by a nearby w_k. Second, they suggest that the input terminals should draw a negligible amount of DC current; hence, if we used a resistive divider to implement the weighted summation, then we would need to buffer the input voltages into the resistive network. In practice, we obtain the most accurate ratios of weighing coefficients by connecting an integral number of unit cells, each with weight *w*, in parallel. In such cases, we are interested primarily in the number of cells rather than the actual weight value involved; in such cases, we omit the *w* associated with each of these amplifier symbols.

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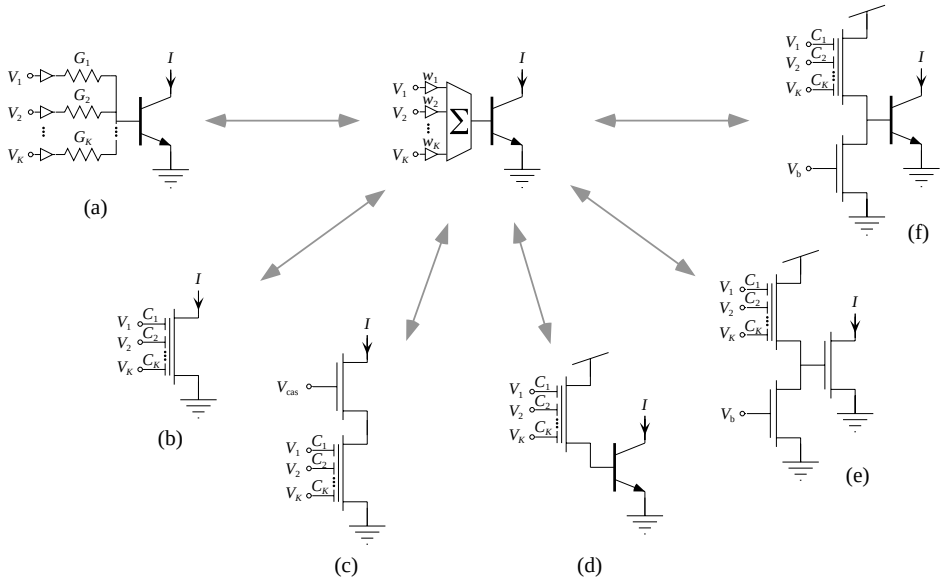

Figure 2. Six implementations of the ideal MITE comprising (a) a resistive voltage divider and a bipolar transistor, (b) a single subthreshold floating-gate MOS (FGMOS) transistor, (c) a cascoded subthreshold FGMOS transistor, (d) a subthreshold FGMOS transistor and a bipolar transistor, (e) a floating-gate source follower and a subthreshold MOS transistor, and (f) a floating-gate source follower and a bipolar transistor. For the five MITE implementations shown in parts b through f, we can use the amount of floating-gate charge to store electronically adjustable, nonvolatile multiplicative scale factors that we can use to build adaptive systems or to compensate for device mismatch.

Without loss of generality, we assume that the weighted summation of the input voltages, U, is of the form

$$U = \sum_{k=1}^{K} w_k V_k,$$

where V_k is the kth input voltage, and w_k is a dimensionless positive weighting coefficient that scales V_k. Further, we assume that the output current, I, is of the form

$$I = \lambda I_s \exp\left[\sum_{k=1}^{K} \frac{w_k V_k}{U_T}\right], \qquad (1)$$

where I_s is a pre-exponential scaling current, which could be temperature dependent, λ is a dimensionless quantity that scales I_s proportionally, and U_T is the thermal voltage, $\frac{kT}{q}$. Note that, if the weighted summation, U, included a voltage offset term, the form of the output current would remain unchanged.

As just defined, the MITE does indeed have K different transconductances, g_1 through g_K, each of which is linear in the output current, I. To demonstrate this property, we simply differentiate Eq. 1 with respect to V_k as follows:

$$\begin{aligned} g_k &= \frac{\partial I}{\partial V_k} \\ &= \frac{w_k}{U_T} \lambda I_s \exp\left[\sum_{k=1}^{K} \frac{w_k V_k}{U_T}\right] \\ &= \frac{w_k}{U_T} I. \end{aligned}$$

3. MULTIPLE-INPUT TRANSLINEAR ELEMENT IMPLEMENTATIONS

Figure 2 shows six different implementations of the MITE. For the first of these MITEs, shown in Fig. 2a, we use a resistive voltage divider to implement the weighted voltage summation and a bipolar transistor to implement the exponential voltage-to-current transduction. In this case, the weighting coefficient associated with each input is inversely proportional to the resistance through which the input couples into the base of the bipolar. We must buffer the input voltages into the resistive network so, in a circuit, the network neither supplies current to, nor sinks current from the input nodes. This resistor-bipolar circuit is only a good MITE implementation over those collector currents for which the base impedance of the bipolar transistor is much greater than the resistances in the resistive network. When the base impedance becomes comparable to the resistances in the resistor network, the base voltage is clamped by the base-emitter junction and the collector current then increases only linearly, instead of exponentially, with the input voltages.

In subthreshold, the drain current of the K-input floating-gate MOS (FGMOS) transistor is proportional to the exponential of a weighted sum of its K control-gate voltages [8]. Consequently, we can implement a MITE using a single subthreshold FGMOS transistor, as shown in Fig. 2b. In this case, the weighting coefficient of each input is proportional to the capacitance through which the input couples into the floating gate. Figure 3 shows experimental measurements from a

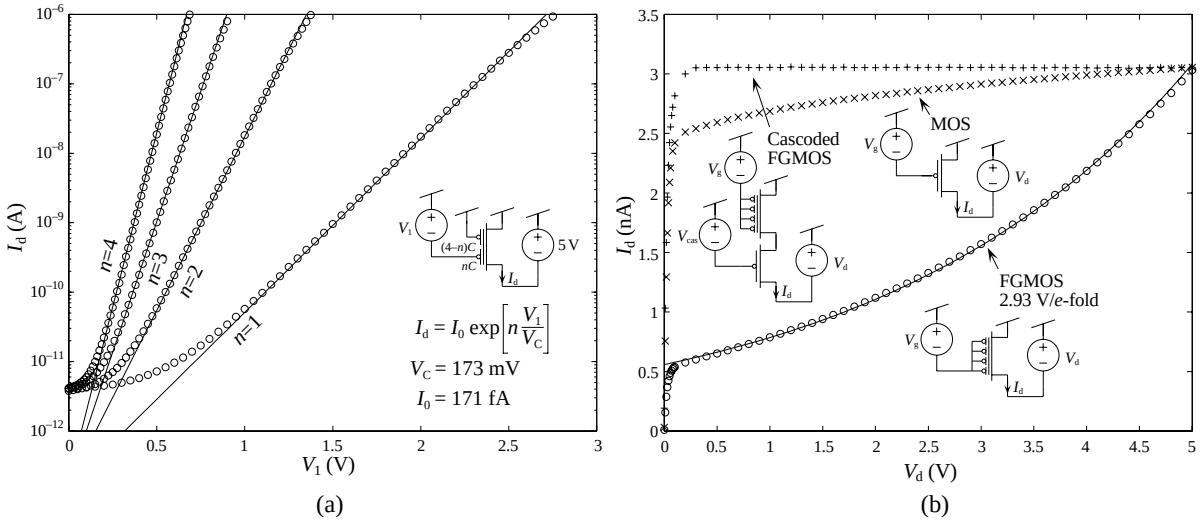

Figure 3. Measured subthreshold current–voltage characteristics from a four-input *p*FGMOS transistor with four nominally identical control gates. (a) The plot shows drain current as a function of control-gate voltage, measured as we swept n of the control gates together with the remaining control gates connected to V_{dd}. (b) Drain current as a function of drain voltage for a subthreshold *p*FGMOS transistor, a subthreshold *p*MOS transistor, and a cascoded subthreshold *p*FGMOS transistor illustrating the effect of the parasitic drain-overlap capacitance on drain conductance.

*p*FGMOS transistor with four nominally identical control gates that we fabricated in a 2–µm double-poly CMOS process. Figure 3a shows drain current measured as a function of control-gate voltage as we swept n of the four control gates together with the remaining ones connected to V_{dd} along with a fit to the data of the form of Eq. 1. The subthreshold FGMOS transistor is a good MITE implementation over currents ranging from 1 pA to about 1 µA.

The main limitation of the single subthreshold FGMOS transistor as a MITE implementation is illustrated in Fig. 3b. The circles in Fig. 3b show measured values of drain current as a function of drain voltage for the four-input *p*FGMOS transistor. As the drain voltage increases beyond 100 mV, the *p*FGMOS transistor "saturates," yet the drain current increases increases exponentially by a factor of six as the drain voltage increases to 5 V. During fabrication, the source and drain implants of an MOS transistor diffuse slightly under the gate, creating a small parasitic capacitance coupling both the source and the drain to the gate. Because the gate of an FGMOS transistor is floating, an increase in the drain voltage couples into the floating gate, thereby increasing the subthreshold drain current exponentially. In principle, we can decrease this coupling as much as we like by making the FGMOS transistor narrower (thereby decreasing the overlap capacitance) or by making the control-gate capacitances larger (thereby increasing the total floating-gate capacitance and, hence, decreasing the drain capacitive-divider ratio), or by using both techniques. However, in practice, neither of these solutions are attractive.

A better solution to this problem is to cascode the subthreshold FGMOS transistor, as shown in Fig. 2c. We can think of the cascode transistor as a source follower with a constant input voltage, V_{cas}; thus, it fixes the drain voltage of the FGMOS transistor (i.e., the source follower's output voltage), effectively reducing the change in current through both transistors resulting from a change in the drain voltage of the cascode transistor. The pluses in Fig. 3b show measured values of drain current as a function of drain voltage for a cascoded four-input subthreshold *p*FGMOS transistor. Once the cascoded *p*FGMOS transistor is saturated (after about 0.3 V), the current–voltage characteristic is flat to within 0.1 %, making the cascoded subthreshold FGMOS transistor a good MITE implementation.

Figure 2d depicts a two-transistor MITE implementation comprising a K-input subthreshold FGMOS transistor and a bipolar transistor. Intuitively, this bipolar-FGMOS MITE implementation works as follows. The subthreshold FGMOS transistor makes a current that is exponential in the weighted sum of the input voltages; again, the weighting coefficient of each input is proportional to the capacitance through which the input couples into the floating gate. The bipolar transistor then acts as a current-gain stage by multiplying the subthreshold FGMOS transistor current by the bipolar's forward current gain. Because the drain of the FGMOS transistor is held at a fixed potential, this MITE implementation is insensitive to the parasitic drain-overlap capacitance.

Figure 4 shows measured data from a four-input version of the circuit of Fig. 2d that we fabricated in a 2–µm double-poly CMOS process. The circles in Fig. 4 show collector current measured as a function of control-gate voltage as we swept n of the four inputs together with the remaining ones grounded. The solid lines show least-squares best-fit lines to the log of the collector current. Note that the slopes, which are indicated along with each curve in Fig. 4, are nearly in a ratio of

1:2:3:4, which is what we expect from Eq. 1. This two-transistor circuit is a good MITE implementation over approximately 7.5 decades of collector current.

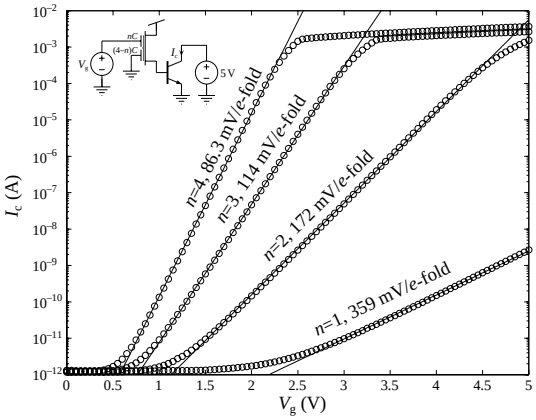

Figure 4. Measured current–voltage characteristics from a four-input version of the MITE implementation of Fig. 2d with four nominally identical weighting coefficients. The plot shows collector current as a function of input voltage, measured as we swept *n* of the inputs together with the remaining inputs grounded.

The final two MITE implementations, shown in Figs. 2e and 2f, are similar—each comprises a two-transistor FGMOS source follower and a third transistor that has an exponential current–voltage characteristic. Intuitively, the floating-gate voltage develops as a weighted sum of the *K* input voltages via a capacitive voltage divider. In the source-follower configuration, the FGMOS transistor's source voltage is approximately a linear function of the floating-gate voltage. Consequently, the source voltage is also a weighted sum of the input voltages. The third transistor then generates a current that is exponential in this source voltage. In the MITE of Fig. 2e, the exponential element is a subthreshold MOS transistor, whereas, in that of Fig. 2f, the exponential element is a bipolar transistor. Because the drains of the FGMOS transistors are held at a fixed potential, these MITE implementations do not suffer from the drain-overlap capacitance problem.

Because the source-follower circuit configuration does not depend on the form of the current–voltage relationship of the MOS transistor, these three-transistor circuits are good MITE implementations even when we bias the FGMOS source follower with an above-threshold current. For the circuit of Fig. 2e, biasing the FGMOS source follower with an above-threshold current allows us to make the output MOS transistor as wide as necessary to get a larger range of exponential currents without having to make the FGMOS transistor, and, hence, the floating-gate capacitance large. The above-threshold bias gives the FGMOS source follower enough bandwidth to drive the large gate capacitance of a wide output MOS transistor. The circuit of Fig. 2f is a valid MITE implementation only when the base current is negligible compared with the source-follower bias current. Thus, for the circuit of Fig. 2f, biasing the FGMOS source follower with above-threshold currents allows us to operate this MITE at high current levels and, thus, potentially with very high bandwidths.

For each of the five FGMOS-transistor–based MITE implementations just described, we can use the floating-gate charge to store adaptable weights for building learning systems or to compensate for scale-factor errors resulting from device mismatch. None of the FGMOS-based MITE implementations, except for the single subthreshold FGMOS transistor, is affected adversely by the parasitic source/drain-overlap capacitances.

4. CONCLUSIONS

In this paper, we defined the MITE, a new circuit primitive from which we can construct low-voltage translinear circuits and log-domain filters. We briefly discussed the operation of six different MITE implementations and showed experimental data from two of these six that we fabricated in a 2–µm double-poly CMOS process.

5. ACKNOWLEDGMENTS

This work is supported in part by the Center for Neuromorphic Systems Engineering as a part of the National Science Foundation Engineering Research Center Program. We would like to thank Carver Mead for both his encouragement of and his generous support for this work.

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