Carl Ebeling
December 1999

Personal

Born January 9, 1950.
Married to Lynne A. Auld, two children.

Education

Ph.D.	Computer Science Carnegie-Mellon University, Pittsburgh, Pa. Dissertation: *All the Right Moves: A VLSI Architecture for Chess.*	1986
M.S.	Computer Science Southern Illinois University, Carbondale, Ill. Thesis: *A User Oriented Microprogramming System.* Supervised by Prof. Ratan Guha.	1976
B.S.	Physics Wheaton College, Wheaton, Ill.	1971

Employment

University of Washington
Department of Computer Science and Engineering

Assistant Professor	1986-92
Associate Professor	1992-97
Professor	1997-

Research Interests

Special-purpose computer architectures; configurable computing architectures; FPGAs; VLSI systems design; computer-aided design of digital systems.

Awards

IBM Doctoral Fellowship	1985
Association for Computing Machinery Distinguished Dissertation Award	1986
National Science Foundation Presidential Young Investigator	1987
American Association for Artificial Intelligence Pioneer in Computer Chess	1989
Burlington Resources Foundation Faculty Achievement Award for Teaching, College of Engineering	1992
Fulbright Fellowship Lecturing at the University of Mauritius	1993-94
University of Washington Distinguished Teaching Award	1995
Allen Newell Award for Research Excellence, for computer chess (Hitech)	1997

Selected Grants

National Science Foundation 1987-92
Presidential Young Investigator, Grant No. CCR-8657589, $282,900.

DARPA 1988-90
Larry Snyder, Principal Investigator (with Gaetano Borriello and Martine Schlag), *VLSI Architectures and CAD*, $1,787,419.

National Science Foundation 1991-92
Co-Principal Investigator (with Gaetano Borriello and Larry Snyder), Grant No. MIP-9013274, *An Inquiry into Chaotic Routing*, $219,837.

DARPA 1991-94
Co-Principal Investigator (with Gaetano Borriello and Larry Snyder), *Synthesis of Timing-Constrained VLSI Systems*, $1,610,495.

National Science Foundation 1993-97
Co-Principal Investigator (with Larry Snyder), Grant No. MIP-9213469, *Chaotic Routing: Study and Implementation*, $1,120,998.

ARPA 1994-98
Co-Principal Investigator (with Gaetano Borriello and Steven Burns), *High-Performance Embedded Systems: From Specification to Implementation*, $1,584,058.

National Science Foundation 1999-02
Co-Principal Investigator (with Hui Liu), *An Experimental Configurable Computing System for Wireless Communication*, $1,009,466.

Patents

Carl Ebeling, Gaetano Borriello, Scott Hauck and Steve Burns. "A Dynamically Reconfigurable Logic Array for Digital Logic Circuits," U. S. Patent #5,208,491. 1993.

Scott Hauck, Gaetano Borriello, Steve Burns, and Carl Ebeling. "A Field-Programmable Gate Array for Synchronous and Asynchronous Operation," U. S. Patent #5,367,209. 1994.

Carl Ebeling, Darren Cronquist and Paul Franklin. "A Configurable Architecture for Pipelined Computation", U. S. Patent issued 1999.

Professional Activities

Member of the Steering Committee, VLSI Educator's Conference, 1988.

Member of the IEEE Awards Paper Committee, 1989-1992.

Member of the NSF Presidential Young Investigator Selection Panel, 1990, 1994.

Member, Program Committee, Conference on Advanced Research in VLSI, March 1991.

Member, Program Committee, Microelectronics Education Conference, July 1991.

Co-Chair, Program Committee, Conference on Advanced Research in VLSI, March 1993.

Member, Program Committee, ACM Symposium on Field-Programmable Gate Arrays, 1992, 1994-2000.

Chair, Program Committee, Fourth ACM Symposium on Field-Programmable Gate Arrays, February 1996.

Member, Program Committee, International Conference on Computer Design, November, 1995, 1996.

Member, Program Committee, 17th Conference on Advanced Research in VLSI, September 1997.

Ph.D. Students Supervised

Brian Lockyear (1994) *Algorithms for Retiming Level-Clocked Circuits* (Synposys)

Scott Hauck (1995) *Multi-FPGA Systems* (co-supervised with Gaetano Borriello) (Northwestern University)

Neil McKenzie (1996) CRANIUM: *A Multicomputer Network Interface for High-Performance User-Level Communication* (Mitsubishi Eastern Research Lab)

Soha Hassoun (1997) *Architectural Retiming: A Technique for Pipelining Latency-Constrained Circuits* (Tufts University)

Darren Cronquist (1999) *Architecture and Programming for the RaPiD Configurable Computing Array* (HP Labs)

Selected Publications

Carl Ebeling and Ofer Zajicek. Validating VLSI Circuit Layout by Wirelist Comparison. In *Proceedings of the IEEE International Conference on Computer Aided Design (ICCAD-83)*, pp. 172-173, September 1983.

Carl Ebeling. *All the Right Moves: A VLSI Architecture for Chess*. The MIT Press, 1986. (ACM Distinguished Dissertation Series.)

Hans Berliner and Carl Ebeling. Pattern Knowledge and Search: The SUPREM Architecture. *Artificial Intelligence*, 38 (2), pp. 161-198, January 1989.

Robert Bedichek, Carl Ebeling, Georges Winkenbach, and Tony DeRose. Rapid Low-Cost Display of Spline Surfaces. In *Proceedings of the Conference on Advanced Research in VLSI*, pp. 340-355. The MIT Press, March 1991.

Scott Hauck, Gaetano Borriello, and Carl Ebeling. TRIPTYCH: An FPGA Architecture with Integrated Logic and Routing. In *Proceedings of the Brown/MIT Conference on Advanced Research in VLSI and Parallel Systems*, pp. 26-43, March 1992.

Brian Lockyear and Carl Ebeling. Optimal Retiming of Multi-Phase, Level-Clocked Circuits. In *Proceedings of the Brown/MIT Conference on Advanced Research in VLSI and Parallel Systems*, pp. 265-280, March 1992.

Miles Ohlrich, Carl Ebeling, Eka Ginting and Lisa Sather. SubGemini: Identifying Subcircuits Using a Fast Subgraph Isomorphism Algorithm. In *Proceedings of the 30th Design Automation Conference*, Dallas, pp. 131-137, June 1993.

Brian Lockyear and Carl Ebeling. Optimal Retiming of Level-Clocked Circuits Using Symmetric Clock Schedules. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 9, pp. 1097-1109, September 1994.

Scott Hauck, Gaetano Borriello, Steven Burns, Carl Ebeling. The Triptych FPGA Architecture. *IEEE Transactions on VLSI Systems*, Vol. 3, No. 4, pp. 491-501, December 1995.

Carl Ebeling, Larry McMurchie, Scott Hauck, Steven Burns. Placement and Routing Tools for the Triptych FPGA. *IEEE Transactions on VLSI Systems*, Vol. 3, No. 4, pp. 473-482, December 1995.

Carl Ebeling and Larry McMurchie. Pathfinder: A Negotiation-Based Router for Routing-Constrained FPGAs. In *Proceedings of the Third ACM Symposium on Field-Programmable Gate Arrays*, Monterey, pp. 111-117, February 1995.

Soha Hassoun and Carl Ebeling. Architectural Retiming: Pipelining Latency-Cosntrained Circuits. In *Proceedings of the Design Automation Conference*, Las Vegas, pp. 708-713, June 1996.

Soha Hassoun and Carl Ebeling. Using Precomputation in Architecture and Logic Resynthesis, In *Proceedings of the International Conference on Computer-Aided Design*, Santa Clara, November, 1998.

Darren Cronquist, Paul Franklin, Miguel Figueroa, and Carl Ebeling. Architecture Design of Reconfigurable Pipelined Datapaths. In *Proceedings of the Conference on Advanced Research in VLSI*, Atlanta, April 1999.