Susan J. Eggers

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Research Interests

Computer architecture and compiler optimization, with an emphasis on experimental performance analysis. Current work is on issues in processor design (multithreaded architectures) and compiler optimizations (dynamic compilation and synchronization in Java).

Education

1992: Ph.D., Computer Science, University of California, Berkeley

1965: B.A, Economics., Connecticut College

Recent Employment

1999 to present: Full Professor, Department of Computer Science and Engineering, University of Washington

1994 to 1999: Associate Professor, Department of Computer Science and Engineering, University of Washington

1989 to 1994: Assistant Professor, Department of Computer Science and Engineering, University of Washington

1984 to 1989: Research assistant, SPUR Multiprocessor Group, Computer Science Division (EECS), University of California, Berkeley

1979 to 1983: Computer Scientist, Department of Computer Science and Mathematics, Lawrence Berkeley Laboratory

Selected Publications

B. Grant, M. Mock, M. Philipose, C. Chambers and S.J. Eggers, "DyC: An Expressive Annotation-Directed Compiler for C", *Theoretical Computer Science* (to appear).

J. Aldrich, C. Chambers, E.G. Sirer and S. Eggers, "Static Analyses for Eliminating Unnecessary Synchronization from Java Programs", Sixth International Static Analysis Symposium (September 1999). pp. 19-38.

J.L. Lo, S.S. Parekh, S.J. Eggers, H.M. Levy and D.M. Tullsen, "Software-Directed Register Deallocation for SMT Processors", *IEEE Transactions on Parallel and Distributed Systems* (September 1999). pp. 922-933.

B. Grant, M. Philipose, M. Mock, C. Chambers and S.J. Eggers, "An Evaluation of Staged Run-time Optimizations", *Conference on Programming Language Design and Implementation* (May 1999), pp. 293-304.

D.M. Tullsen, J.L. Lo, S.J. Eggers and H.M. Levy, "Supporting Fine-Grain Synchronization on a Simultaneous Multithreaded Processor", *Fifth International Conference on High-Performance Computer Architecture* (January 1999), pp. 54-58.

J.L. Lo, L. Barroso, S.J. Eggers, K. Gharachorloo, H.M. Levy and S.S. Parekh, "An Analysis of Database Workload Performance on Simultaneous Multithreaded Processors", *International Symposium on Computer Architecture* (June, 1998), pp 39-50.

J.L. Lo, S.J. Eggers, H.M. Levy, S.S. Parekh and D.M. Tullsen, "Tuning Compiler Optimizations for Simultaneous Multithreading," *International Symposium on Microarchitecture* (December, 1997), pp. 114-124. Chosen for a special edition of *International Journal of Parellel Processing* (to appear).

S.J. Eggers, J.S. Emer, H.M. Levy, J.L. Lo, R.L. Stamm and D.M. Tullsen, "Simultaneous Multithreading: A Platform for Next-generation Processors," *IEEE Micro* (September/October, 1997), pp. 12-19.

J.L. Lo, S.J. Eggers, J.S. Emer, H.M. Levy, R.L. Stamm and D.M. Tullsen, "Converting Thread-level Parallelism into Instruction-level Parallelism via Simultaneous Multithreading," *ACM Transactions on Computer Systems* (August, 1997), pp. 322-354.

B. Grant, M. Mock, M. Philipose, C. Chambers and S.J. Eggers, "Annotation-directed Run-time Specialization in C," *Symposium on Partial Evaluation and Semantics-based Program Manipulation* (June, 1997), pp. 163-178.

D.M. Tullsen, S.J. Eggers, J.S. Emer, H.M. Levy, J.L. Lo, and R.L. Stamm, "Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreading Processor", *International Symposium on Computer Architecture* (May, 1996), pp 191-202.

J. Auslander, M. Philipose, C. Chambers, S.J. Eggers and B.N. Bershad, "Fast, Effective Dynamic Compilation", *Conference on Programming Language Design and Implementation* (May, 1996), pp. 149-159.

B.N. Bershad, S. Savage, P. Pardyak, E.G. Sirer, M. Fiuczynski, D. Becker, S. Eggers and C. Chambers, "Extensibility,

Safety and Performance in the SPIN Operating System," *Symposium on Operating Systems Principles* (November, 1995), pp. 267-284.

T.E. Jeremiassen and S.J. Eggers, "Reducing False Sharing on Shared Memory Multiprocessors through Compile Time Data Transformations," *Symposium on Principles and Practice of Parallel Programming* (July, 1995), pp. 179-188.

D.M. Tullsen, S.J. Eggers and H.M. Levy, "Simultaneous Multithreading: Maximizing On-chip Parallelism," *International Symposium on Computer Architecture* (June, 1995), pp 392-403. Selected for the 25th Anniversary Anthology.

J.L. Lo and S.J. Eggers, "Improving Balanced Scheduling with Compiler Optimizations that Increase Instruction-level Parallelism," *International Symposium on Programming Language Design and Implementation* (June, 1995), pp. 151-162.

D.M. Tullsen and S.J. Eggers, "Effective Cache Prefetching on a Bus-Based Multiprocessor," *ACM Transactions on Computer Systems* (February, 1995), pp. 57-88.

R. Thekkath and S.J. Eggers, "The Effectiveness of Multiple Hardware Contexts," *International Conference on Architectural Support for Programming Languages and Operating Systems* (October, 1994), pp. 328-337.

T.E. Jeremiassen and S.J. Eggers, "Static Analysis of Barrier Synchronization in Explicitly Parallel Programs," *International Conference on Parallel Architecture and Compilation Techniques* (August, 1994), pp. 171-180.

R. Thekkath and S.J. Eggers, "Impact of Sharing-Based Thread Placement on Multithreaded Architectures," *International Symposium on Computer Architecture* (April, 1994), pp. 176-186.

D. Kerns and S.J. Eggers, "`Balanced Scheduling: Instruction Scheduling When Memory Latency is Uncertain" *Conference on Programming Language Design and Implementation* (June, 1993), pp. 278-289.

D.M. Tullsen and S.J. Eggers, "Limitations of Cache Prefetching in Shared Memory Multiprocessors," *International Symposium on Computer Architecture* (May, 1993), pp. 278-288.

E.J. Koldinger, J.S. Chase and S.J. Eggers, "Architectural Support for Single Address Space Operating Systems," *International Conference on Architectural Support for Programming Languages and Operating Systems* (October, 1992), pp. 175-186.

S.J. Eggers, "Simplicity Versus Accuracy in a Model of Cache Coherency Overhead", *IEEE Transactions on Computers*, 40:8 (August, 1991), pp. 893-906.

D.G. Bradlee, R.R. Henry and S.J. Eggers, "The Marion System for Retargetable Instruction Scheduling", *Conference on Programming Language Design and Implementation* (June, 1991), pp. 229-240.

E.J. Koldinger, S.J. Eggers and H.M. Levy, "On the Validity of Trace-Driven Simulation for Multiprocessors", *International Symposium on Computer Architecture* (May, 1991), pp. 244-253.

D.G. Bradlee, S.J. Eggers and R.R. Henry, "Integrating Register Allocation and Instruction Scheduling for RISCs", *International Conference on Architectural Support for Programming Languages and Operating Systems* (April, 1991), pp. 122-131.

S.J. Eggers, D. Keppel, E. Koldinger and H.M. Levy, "Techniques for Inline Tracing on a Shared-memory Multiprocessor", *ACM SIGMETRICS Conference on Measurement and Modeling of Computer Systems* (May, 1990), pp. 37-47.

S.J. Eggers and R.H. Katz, "Evaluating the Performance of Four Snooping Cache Coherency Protocols", *International Symposium on Computer Architecture* (June, 1989), pp. 2-15.

S.J. Eggers and R.H. Katz, "The Effect of Sharing on the Cache and Bus Performance of Parallel Programs", *International Conference on Architectural Support for Programming Languages and Operating Systems* (April, 1989), pp. 257-270.

S.J. Eggers and R.H. Katz, "A Characterization of Sharing in Parallel Programs", *International Symposium on Computer Architecture* (June, 1988), pp. 373-382.

M. Hill, S. Eggers, J. Larus, G. Taylor, G. Adams, B.K. Bose, G. Gibson, P. Hansen, J. Keller, S. Kong, C. Lee, D. Lee, J. Pendleton, S. Ritchie, D. Wood, B. Zorn, P. Hilfinger, D. Hodges, R. Katz, J. Ousterhout and D. Patterson, "Design Decisions in SPUR", *IEEE Computer,* Vol. 19, No. 10 (November, 1986), pp. 8-22.

D.A. Wood, S.J. Eggers, G. Gibson, M.D. Hill, J.M. Pendleton, S.A. Ritchie, G.S. Taylor, R.H. Katz and D.A. Patterson, "An In-Cache Address Translation Mechanism", *International Symposium on Computer Architecture* (June,

1986), pp. 358-365.

Thesis Students

Doctoral Students: David Bradlee (Microsoft), Tor Jeremiassen (Bell Laboratories, Lucent Technologies), Jack Lo (Transmeta, Inc.), David Keppel (Transmeta, Inc.), Radhika Thekkath (MIPS, Inc.), Dean Tullsen (University of California, San Diego)

Postdoctoral Fellow: Wilson Hsieh (University of Utah)

A total of 10 graduated doctoral and masters students, 8 current graduate students, 1 postdoctoral fellow.

Grants

National Science Foundation, Staged Optimization, $500,000, Co-PI, 1999-2001.

National Science Foundation, Simultaneous Multithreading, $807,790, Co-PI, 1996-1999.

Office of Naval Research, Dynamic Compilation, $380,664, Co-PI, 1996-1999.

Advanced Research Projects Agency, Application-Specific Operating Systems for High-Performance Computing, $3,096,620, Co-PI, 1994-1997.

Intel, Memory Management for Advanced Processors, $761,620 (100% allowance on equipment), Co-PI, 1994-1995.

Office of Naval Research, Compiler Reorganization of Shared Data, $402,994, PI, 1992-1995.

National Science Foundation: Career Advancement Award for Women Scientists and Engineers, Code Scheduling under Varying Parallel Resource Constraints, $49,999, PI, 1992-1993.

AT&T Bell Laboratories, PYI Matching Program, $75,000, PI, 1991-1994.

Washington Technology Center, Compiler Support for Complex Parallel Hardware, $25,000, PI, 1990-1991.

International Business Machines, Better Multiprocessor Cache Performance in Software-Managed Caches through Compiler Reorganization of Shared Memory, $110,807, PI, 1990-1991.

Sun Microsystems, equipment gift, $100,850, PI, 1990.

Sun Microsystems, equipment gift, $304,850, PI, 1990.

University of Washington: Faculty Workstation Initiative, equipment gift, $3,500, PI, 1990.

International Business Machines: Faculty Development Award, $60,000, PI, 1989-1991.

University of Washington: Graduate School Research Fund, Measuring Coherency-related Processor Delay in Parallel Programs, $8,944, PI, 1989.

Awards

AT&T Bell Laboratories, PYI Matching Program, 1991-1994.

National Science Foundation: Presidential Young Investigator Award, 1990-1995.

International Business Machines: Faculty Development Award, 1989-1991.

International Business Machines: Graduate Fellowship, 1986-1988.

California Fellowship in Microelectronics, 1985-1986.

Selected Professional Activities

CRA Workshop on Academic Careers in Computer Science, Panel Chair, 1999, 1997, 1996, 1994, 1993.

Workshop on Compiler Support for System Software, Program Committee, 1999.

International Conference on Architectural Support for Programming Languages and Operating Systems, Program Chair, 1996; Program Committee, 1994 & 1992.

NSF Workshop on Critical Issues in Computer Architecture, Steering Committee, 1996.

CRAW Faculty Mentoring Program, Steering Committee, 1995.

Symposium on Computer Architecture, Program Committee, 1995, 1990.

ARPA Compiler Infrastructure Workshop (which led to the DARPA/NSF NIS program), Panel Member, 1995 & 1993.

SIGPLAN ‘93 Conference on Programming Language Design and Implementation, Program Committee, 1993 & 2000.

Letters on Programming Languages and Systems, Editor, 1996 - 1993.

NSF Workshop on Memory Latency, Panel Member, 1993.

NSF Workshop on Experimental Research, Panel Member, 1991.