Prof. Luis Ceze

Computer Science and Engineering
University of Washington
Paul G. Allen Center, Office #576
185 Stevens Way
Seattle, WA, 98195-2350
(206) 543-1896 (Office)

luisceze@cs.washington.edu
http://www.cs.washington.edu/homes/luisceze
http://sampl.ai
http://misl.bio

RESEARCH INTERESTS

Intersection between computer architecture, programming languages, machine learning and biology. Current focus is on approximate computing, hardware/software co-design by and for machine learning, and DNA-based data storage and processing.

EMPLOYMENT/APPOINTMENTS

- **Computer Science and Engineering, University of Washington**, Seattle, WA.
  Full Professor, September 2017-present.
  Associate Professor, September 2012-August 2017.
  Assistant Professor, September 2007-August 2012.
- **OctoML, Inc.**, Seattle, WA.
  Co-founder and CEO, July 2019-present.
- **Madrona Venture Group**, Seattle, WA.
  Venture Partner, February 2018-present.
- **Computer Laboratory, University of Cambridge**, Cambridge, UK.
  Visiting Scholar, July 2013-December 2013.
- **Computer Science Department, University of Illinois at Urbana Champaign**, Urbana, IL.
  Research Assistant, August 2002-July 2007.
- **IBM Research**,Yorktown Heights, NY.
  Research Intern/Co-op, June 2001-July 2002, Summers of 2003, 2004, 2006.

EDUCATION

- **University of Illinois at Urbana Champaign (UIUC)**, Urbana, IL.
  Ph.D. in Computer Science, July 2007.
  Thesis: *Bulk Operation and Data Coloring for Multiprocessor Programmability*

- **University of São Paulo, Polytechnic School**, Brazil.
  M.Eng. in Electrical Engineering, August 2002
  Thesis: *BGLsim, Complete System Simulator for Blue Gene/L*

- **University of São Paulo, Polytechnic School**, Brazil.
  B.S. in Electrical Engineering, December 2000

SELECTED AWARDS AND HONORS

- **2021** Lazowska Endowed Professorship
- **2020** ACM SIGARCH Maurice Wilkes Award

- ◇ **2018** Cover Feature in Nature Biotechnology
- ◇ **2018** Paper selected for the IEEE Micro Top Picks as Honorable Mention
- ◇ **2017** Paper selected for the IEEE Micro Top Picks
- ◇ **2016** DNA data storage project featured in The Future of Everything by Wall Street Journal
- ◇ **2016** DNA data storage project selected as Best of What's New by Popular Science
- ◇ **2016** Paper selected for the IEEE Micro Top Picks as Honorable Mention
- ◇ **2015** UIUC Distinguished Alumni Educator Award
- ◇ **2015** USENIX'15 ATC Best Paper Award
- ◇ **2015** Received the Torode Family Career Development Professorship
- ◇ **2014** Paper selected as CACM Research Highlight
- ◇ **2013** IEEE TCCA Young Computer Architect Award
- ◇ **2013** Paper selected for the IEEE Micro Top Picks
- ◇ **2010** Kavli Frontiers of Science Fellow
- ◇ **2010** UW CSE ACM Undergraduate Teacher of the Year Award
- ◇ **2010** Sloan Research Fellowship
- ◇ **2009** Paper selected for the IEEE Micro Top Picks, Jan/Feb 2010
- ◇ **2009** Microsoft New Faculty Fellowship
- ◇ **2009** NSF CAREER Award
- ◇ **2008** Two papers selected for the IEEE Micro Top Picks, Jan/Feb 2009
- ◇ **2008** Paper selected from ISCA'08 to appear in Communications of ACM
- ◇ **2008** David J. Kuck Outstanding Thesis Award, UIUC
  - · Given by the Department of Computer Science to one thesis per year to recognize quality and impact. (The thesis was also nominated by UIUC for the ACM Doctoral Dissertation Award.)
- ◇ **2007** Ross J. Martin Award, UIUC
  - · Given by the College of Engineering to recognize outstanding research achievement
- ◇ **2006** CW Gear Outstanding Graduate Student Award, UIUC
  - · Given by the CS Department to one outstanding graduate student each year
- ◇ **2005** Paper selected for the IEEE Micro Top Picks, Jan/Feb 2006
- ◇ **2005** WJ Poppelbaum Memorial Award, UIUC
  - · For academic merit and creativity in computer architecture
- ◇ **2004** IBM Outstanding Internship Award
- ◇ **2004-2005** IBM PhD Fellowship
- ◇ **2003** Distinguished Paper, EuroPar 2003
- ◇ **2002** IBM Bravo! Award for the contribution to the Blue Gene/L project.

SELECTED REFEREED PUBLICATIONS

Google Scholar search link: `http://bit.ly/2tBimMX`

1. Bojian Zheng nd Ziheng Jiang, Cody Hao Yu, Haichen Shen, Josh Fromm, Yizhi Liu, Yida Wang, Luis Ceze, Tianqi Chen, and Gennady Pekhimenko. Diefcode: Automatic ooptmization for dynamic tensor programs. In *Proceedings of the MLSys Conference*, 2022
2. Liang Luo, Peter West, and Pratyush Patel nd Arvind Krishnamurthy nd Luis Ceze. Srifty: A throughput and cost optimizer for public cloud-based distributed training. In *Proceedings of the MLSys Conference*, 2022

3. Bichlien H. Nguyen, Christopher N. Takahashi, Gagan Gupta, Jake A. Smith, Richard Rouse, Paul Berndt, Sergey Yekhanin, David P. Ward, Siena D. Ang, Patrick Garvan, Hsing-Yeh Parker, Rob Carlson, Douglas Carmean, Luis Ceze, and Karin Strauss. Scaling dna data storage with nanoscale electrode wells. *Science advances*, 7, 2021
4. Eddie Yan, Liang Luo, and Luis Ceze. Characterizing and taming resolution in convolutional neural networks. pages 189–200, 2021
5. Nicolas Cardozo, Karen Zhang, Kathryn Doroschak, Aerilynn Nguyen, Zoheb Siddiqui, Nicholas Bogard, Karin Strauss, Luis Ceze, and Jeff Nivala. Multiplexed direct detection of barcoded protein reporters on a nanopore array. *Nature biotechnology*, pages 1–5, 2021
6. Callista Bee, Yuan-Jyue Chen, Melissa Queen, David Ward, Xiaomeng Liu, Lee Organick, Georg Seelig, Karin Strauss, and Luis Ceze. Molecular-level similarity search brings computing to dna data storage. *Nature communications*, 12:1–9, 2021
7. Luis Vega, Joseph McMahan, Adrian Sampson, Dan Grossman, and Luis Ceze. Reticle: a virtual machine for programming modern fpgas. *Proceedings of the 42nd ACM SIGPLAN International Conference on Programming Language Design and Implementation*, pages 756–771, 2021
8. Liang Luo, Jacob Nelson, Arvind Krishnamurthy, and Luis Ceze. Cloud collectives: Towards cloud-aware collectives for ml workloads with rank reordering. *arXiv preprint*, arXiv:2105.14088, 2021
9. Gus Henry Smith, Andrew Liu, Steven Lyubomirsky, Scott Davidson, Joseph McMahan, Michael Taylor, Luis Ceze, and Zachary Tatlock. Pure tensor program rewriting via access patterns (representation pearl). *arXiv preprint*, arXiv:2105.09377, 2021
10. Lee Organick, Bichlien H. Nguyen, Rachel McAmis, Weida D. Chen, A. Xavier Kohll, Siena Dumas Ang, Robert N. Grass, Luis Ceze, and Karin Strauss. An empirical comparison of preservation methods for synthetic dna data storage. *Small Methods*, 5(5):2001094, 2021
11. Chien-Yu Lin, Liang Luo, and Luis Ceze. Accelerating spmm kernel with cache-first edge sampling for gnn inference. *arXiv preprint*, arXiv:2104.10716, 2021
12. Brandon Haynes, Maureen Daum, Dong He, Amrita Mazumdar, Magdalena Balazinska, Alvin Cheung, and Luis Ceze. Vss: A storage system for video analytics. *arXiv preprint*, arXiv:2103.16604, 2021
13. Ziheng Jiang, Animesh Jain, Andrew Liu, Josh Fromm, Chengqian Ma, Tianqi Chen, and Luis Ceze. Automated backend-aware post-training quantization. *arXiv preprint*, arXiv:2103.14949, 2021
14. Karen Zhang, Yuan-Jyue Chen, Kathryn Doroschak, Karin Strauss, Luis Ceze, Georg Seelig, and Jeff Nivala. A nanopore interface for high bandwidth dna computing. *bioRxiv*, 2021
15. Johannes Linder, Yuan-Jyue Chen, David Wong, Georg Seelig, Luis Ceze, and Karin Strauss. Robust digital molecular design of binarized neural networks. *27th International Conference on DNA Computing and Molecular Programming (DNA 27)*, 2021
16. Jason S. Hoffman, Matthew Hirano, Nuttada Panpradist, Joseph Breda, Parker Ruth, Yuanyi Xu, Jonathan Lester, Bichlien H. Nguyen, Luis Ceze, and Shwetak N. Patel. Passively sensing sars-cov-2 rna in public transit buses. *Science of The Total Environment*, page 152790, 2022
17. Claris Winston, Lee Wohlen Organick, Luis H Ceze, Karin Strauss, and Yuan-Jyue Chen. A combinatorial pcr method for efficient, selective oligo retrieval from complex oligo pools. *bioRxiv*, 2021
18. Peter Ney, Lee Organick, Jeff Nivala, Luis Ceze, and Tadayoshi Kohno. Dna sequencing flow cells and the security of the molecular-digital interface. *Proceedings on Privacy Enhancing Technologies*, pages 413–432, 2021
19. Luis Ceze and Karin Strauss. Dna data storage and near-molecule processing for the yottabyte era. pages 417–429, 2021
20. Liang Luo, Peter West, Arvind Krishnamurthy, and Luis Ceze. Srift: Swift and thrift cloud-based distributed training. *arXiv preprint*, (arXiv:2011.14243), 2020
21. Kathryn Doroschak, Karen Zhang, Melissa Queen, Aishwarya Mandyam, Karin Strauss, Luis Ceze, and Jeff Nivala. Rapid and robust assembly and decoding of molecular tags with dna-based nanopore signatures. *Nature Communications*, 11(1):1–9, 2020

22. Josh Fromm, Meghan Cowan, Matthai Philipose, Luis Ceze, and Shwetak Patel. Riptide: Fast end-to-end binarized neural networks. In *Proceedings of the 3rd MLSys Conference*, 2020
23. Liang Luo, Peter West, Jacob Nelson, Arvind Krishnamurthy, and Luis Ceze. Plink: Efficient cloud-based training with topology-aware dynamic hierarchical aggregation. In *Proceedings of the 3rd MLSys Conference*, 2020
24. Peter Ney, Luis Ceze, and Tadayoshi Kohno. Genotype extraction and false relative attacks: Security risks to third-party genetic genealogy services beyond identity inference. In *Network and Distributed System Security Symposium (NDSS)*, volume 10, page 19, 2020
25. Meghan Cowan, Thierry Moreau, Tianqi Chen, James Bornholt, and Luis Ceze. Automatic generation of high-performance quantized machine learning kernels. In *Proceedings of the 18th ACM/IEEE International Symposium on Code Generation and Optimization*, pages 305–316, 2020
26. A. Xavier Kohll, Philipp L. Antkowiak, Weida Chen, Bichlien Nguyen, Wendelin Jan Stark, Luis Ceze, Karin Strauss, and Robert N. Grass. Stabilizing synthetic dna for long-term data storage with earth alkaline salts. *Chemical Communications*, 2020
27. Lee Organick, Yuan-Jyue Chen, Siena Dumas Ang, Randolph Lopez, Xiaomeng Liu, Karin Strauss, and Ceze. Probing the physical limits of reliable dna data retrieval. *Nature communications*, 11(1):1–7, 2020
28. Thierry Moreau, Tianqi Chen, Luis Vega, Jared Roesch, Eddie Yan, Lianmin Zheng, Josh Fromm, Ziheng Jiang, Luis Ceze, Carlos Guestrin, et al. A hardware–software blueprint for flexible deep learning specialization. *IEEE Micro*, 39(5):8–16, 2019. Best paper award
29. Sharon Newman, Ashley P. Stephenson, Max Willsey, Bichlien H. Nguyen, Christopher N. Takahashi, Karin Strauss, and Luis Ceze. High density dna data storage library via dehydration with digital microfluidic retrieval. *Nature communications*, 10(1):1706, 2019
30. Christopher N. Takahashi, Bichlien H. Nguyen, Karin Strauss, and Luis Ceze. Demonstration of end-to-end automation of dna data storage. *Scientific reports*, 9(1):4998, 2019
31. Randolph Lopez, Yuan-Jyue Chen, Siena Dumas Ang, Sergey Yekhanin, Konstantin Makarychev, Miklos Z. Racz, Georg Seelig, Karin Strauss, and Luis Ceze. Dna assembly for nanopore data storage readout. *Nature communications*, 10(1):1–9, 2019
32. Luis Ceze, Jeff Nivala, and Karin Strauss. Molecular digital data storage using dna. *Nature Reviews Genetics*, page 1, 2019
33. Weida D. Chen, A. Xavier Kohll, Bichlien H. Nguyen, Julian Koch, Reinhard Heckel, Wendelin J. Stark, Luis Ceze, Karin Strauss, and Robert N. Grass. Combining data longevity with high storage capacity—layer-by-layer dna encapsulated in magnetic nanoparticles. *Advanced Functional Materials*, page 1901672, 2019
34. Amrita Mazumdar, Brandon Haynes, Magda Balazinska, Luis Ceze, Alvin Cheung, and Mark Oskin. Perceptual compression for video storage and processing systems. In *Proceedings of the ACM Symposium on Cloud Computing*, pages 179–192. ACM, 2019
35. Max Willsey, Ashley Stephenson, Chris Takahashi, Bichlien Nguyen, Karin Strauss, and Luis Ceze. Scaling microfluidics to complex, dynamic protocols. In *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 1–6. IEEE, 2019
36. Max Willsey, Ashley P. Stephenson, Chris Takahashi, Pranav Vaid, Bichlien H. Nguyen, Michal Piszczek, Christine Betts, Sharon Newman, Sarang Joshi, Karin Strauss, and Luis Ceze. Puddle: A Dynamic, Error-Correcting, Full-Stack Microfluidics Platform. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2019
37. D. Carmean, L. Ceze, G. Seelig, K. Stewart, K. Strauss, and M. Willsey. DNA Data Storage and Hybrid Molecular–Electronic Computing. *Proceedings of the IEEE*, 2019
38. Tianqi Chen, Lianmin Zheng, Eddie Yan, Ziheng Jiang, Thierry Moreau, Luis Ceze, Carlos Guestrin, and Arvind Krishnamurthy. Learning to optimize tensor programs. In *Advances in Neural Information Processing Systems (NeurIPS)*, 2018

39. Tianqi Chen, Thierry Moreau, Ziheng Jiang, Lianmin Zheng, Eddie Yan, Haichen Shen, Meghan Cowan, Leyuan Wang, Yuwei Hu, and Luis Ceze. TVM: An Automated End-to-End Optimizing Compiler for Deep Learning. In *Symposium on Operating Systems Design and Implementation (OSDI)*, 2018
40. Lee Organick, Siena Dumas Ang, Yuan-Jyue Chen, Randolph Lopez, Sergey Yekhanin, Konstantin Makarychev, Miklos Z. Racz, Govinda Kamath, Parikshit Gopalan, Bichlien Nguyen, Christopher N. Takahashi, Sharon Newman, Hsing-Yeh Parker, Cyrus Rashtchian, Kendall Stewart, Gagan Gupta, Robert Carlson, John Mulligan, Douglas Carmean, Georg Seelig, Luis Ceze, and Karin Strauss. Random access in large-scale DNA data storage. *Nature Biotechnology*, 2018. ISBN: 1364298980840
41. Kendall Stewart, Yuan-Jyue Chen, David Ward, Xiaomeng Liu, Georg Seelig, Karin Strauss, and Luis Ceze. A content-addressable DNA database with learned sequence encodings. In *International Conference on DNA Computing and Molecular Programming*, pages 55–70. Springer, 2018
42. Liang Luo, Suman Nath, Lenin Ravindranath Sivalingam, Madan Musuvathi, and Luis Ceze. Troubleshooting Transiently-Recurring Errors in Production Systems with Blame-Proportional Logging. In *USENIX Annual Technical Conference (USENIX ATC)*, pages 321–334, 2018
43. Liang Luo, Jacob Nelson, Luis Ceze, Amar Phanishayee, and Arvind Krishnamurthy. Parameter Hub: a Rack-Scale Parameter Server for Distributed Deep Neural Network Training. In *Proceedings of the ACM Symposium on Cloud Computing*, pages 41–54. ACM, 2018
44. M. Willsey, V. T. Lee, A. Cheung, R. Bodík, and L. Ceze. Iterative Search for Reconfigurable Accelerator Blocks with a Compiler in the Loop. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pages 1–1, 2018
45. V. T. Lee, A. Alaghi, R. Pamula, V. S. Sathe, L. Ceze, and M. Oskin. Architecture Considerations for Stochastic Computing Accelerators. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(11):2277–2289, 2018
46. Brandon Haynes, Amrita Mazumdar, Armin Alaghi, Magdalena Balazinska, Luis Ceze, and Alvin Cheung. LightDB: A DBMS for Virtual Reality Video. In *Proceedings of VLDB*, July 2018
47. Sung Kim, Patrick Howe, Thierry Moreau, Armin Alaghi, Luis Ceze, and Visvesh Sathe. MATIC: Learning Around Erros for Efficient Low-Voltage Neural Network Accelerators. In *Design, Automation and Test in Europe*, March 2018. Best paper award
48. Vincent Lee, Armin Alaghi, and Luis Ceze. Correlation Manipulating Circuits for Stochastic Computing. In *Design, Automation and Test in Europe*, March 2018
49. Vincent T. Lee, Amrita Mazumdar, Carlo C. del Mundo, Armin Alaghi, Luis Ceze, and Mark Oskin. Application codesign of near-data processing for similarity search. In *IPDPS*, May 2018
50. Lee Organick, Siena Dumas Ang, Yuan-Jyue Chen, Randolph Lopez, Sergey Yekhanin, Konstantin Makarychev, Miklos Z. Racz, Govinda Kamath, Parikshit Gopalan, Bichlien Nguyen, Christopher Takahashi, Sharon Newman, Hsing-Yeh Parker, Cyrus Rashtchian, Kendall Stewart, Gagan Gupta, Robert Carlson, John Mulligan, Douglas Carmean, Georg Seelig, Luis Ceze, and Karin Strauss. Scaling up dna data storage and random access retrieval. *bioRxiv*, August 2017. Accepted for publication at Nature Biotechnology
51. Cyrus Rashtchian, Konstantin Makarychev, Miklos Racz, Siena Ang, Djordje Jevdjic, Sergey Yekhanin, Luis Ceze, and Karin Strauss. Clustering billions of reads for dna data storage. In *NIPS*, November 2017
52. Thierry Moreau, Joshua S. Miguel, Mark Wyse, James Bornholt, Armin Alaghi, Luis Ceze, Natalie E. Jerger, and Adrian Sampson. A Taxonomy of General Purpose Approximate Computing Techniques. *IEEE Embedded Systems Letters*, October 2017
53. Peter Ney, Karl Koscher, Lee Organick, Luis Ceze, and Tadayoshi Kohno. Computer Security, Privacy, and DNA Sequencing: Compromising Computers with Synthesized DNA, Privacy Leaks, and More. In *USENIX Security*, 2017
54. Eddie Yan, Kaiyuan Zhang, Xi Wang, Karin Strauss, and Luis Ceze. Customizing Progressive JPEG for Efficient Image Storage. In *USENIX HotStorage*, 2017

55. Amrita Mazumdar, Armin Alaghi, Jonathan T. Barron, David Gallup, Luis Ceze, Mark Oskin, and Steven M. Seitz. A Hardware-Friendly Bilateral Solver for Real-Time Virtual Reality Video. In *High Performance Graphics (HPG)*, 2017
56. Vincent T. Lee, Justin Kotalik, Carlo C. del Mundo, Armin Alaghi, Luis Ceze, and Mark Oskin. Similarity Search on Automata Processors. In *International Parallel and Distributed Processing Symposium (IPDPS)*, 2017
57. Amrita Mazumdar, Thierry Moreau, Sung Kim, Meghan Cowan, Armin Alaghi, Luis Ceze, Mark Oskin, and Visvesh Sathe. Exploring computation-communication tradeoffs in camera systems. In *IISWC*, May 2017
58. Brandon Haynes, Artem Minyaylov, Magdalena Balazinska, Luis Ceze, and Alvin Cheung. VisualCloud Demonstration: A DBMS for Virtual Reality. In *SIGMOD*, 2017
59. Margaret E. Morris, Douglas M. Carmean, Artem Minyaylov, and Luis Ceze. Augmenting Interpersonal Communication through Connected Lighting. 2017
60. Vincent Lee, Armin Alaghi, John Hayes, Visvesh Sathe, and Luis Ceze. Energy-Efficient Hybrid Stochastic-Binary Neural Networks for Near-Sensor Computing. In *Design, Automation and Test in Europe*, April 2017
61. Ming Liu, Liang Luo, Jacob Nelson, Arvind Krishnamurthy, and Luis Ceze. IncBricks: Towards In-network Computation with an In-Network Cache. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2017. Selected as Honorable Mention for IEEE Micro Top Picks
62. Djordje Jevdjic, Karin Strauss, Luis Ceze, and Henrique Malvar. Approximate Storage for Encoded and Encrypted Videos. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2017
63. Brandon Holt, James Bornholt, Irene Zhang, Dan R. K. Ports, Mark Oskin, and Luis Ceze. Disciplined Inconsistency with Consistency Types. In *ACM Symposium on Cloud Computing (SOCC)*, 2016
64. James Bornholt, Randolph Lopez, Karin Strauss, Douglas M Carmean, Luis Ceze, Georg Seelig, and Karin Strauss. A DNA-Based Archival Storage System. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2016. Selected for IEEE Micro Top Picks 2016
65. Qing Guo, Karin Strauss, Luis Ceze, and Henrique Malvar. High-Density Image Storage Using Approximate Memory Cells. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2016
66. James Bornholt, Emina Torlak, Dan Grossman, and Luis Ceze. Optimizing synthesis with metasketches. In *POPL*, 2016
67. Adrian Sampson, André Baixo, Benjamin Ransford, Thierry Moreau, Joshua Yip, Luis Ceze, and Mark Oskin. Accept: A programmer-guided compiler framework for practical approximate computing. `http://accept.rocks/`, 2014
68. Luis Ceze and Karin Strauss. The 2014 Top Picks in Computer Architecture. *IEEE Micro*, 35(3), 2015
69. Olivier Temam and Luis Ceze. Alternative Computing Designs and Technologies. *IEEE Micro*, 35(5), 2015
70. Carlo del Mundo, Vincent Lee, Luis Ceze, and Mark Oskin. Ncam: Near-data processing for nearest neighbor search. In *MEMSYS*, 2015
71. Brett Boston, Adrian Sampson, Dan Grossman, and Luis Ceze. Probability type inference for flexible approximate programming. In *OOPSLA*, 2015
72. Adrian Sampson, James Bornholt, and Luis Ceze. "hardware–software co-design: Not just a cliche". In *SNAPL*, 2015
73. Ben Ransford, Adrian Sampson, and Luis Ceze. Approximate Semantics for Wirelessly Networked Applications. In *arxiv*, October 2015. Earlier version appeared in Workshop on Approximate Computing Across the Stack (WACAS w/ ASPLOS) 2014

74. Thierry Moreau, Adrian Sampson, and Luis Ceze. Approximate computing: Making mobile systems more efficient. *Pervasive Computing, IEEE*, April 2015
75. Jacob Nelson, Brandon Holt, Brandon Myers, Preston Briggs, Luis Ceze, Simon Kahan, and Mark Oskin. Latency-Tolerant Software Distributed Shared Memory. In *USENIX Annual Technical Conference (ATC)*, July 2015. Best Paper Award
76. Brandon Holt, Irene Zhang, Dan Ports, Mark Oskin, and Luis Ceze. Claret: Using Data Types for Highly Concurrent Distributed Transactions. In *Workshop on Principles and Practice of Consistency (PaPoC'15 w/ EuroSys)*, April 2015
77. Mike Ringenburg, Adrian Sampson Isaac Ackerman, Luis Ceze, and Dan Grossman. Debugging Approximate Programs via Dynamic Analysis. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2015
78. James Bornholt, Emina Torlak, Luis Ceze, and Dan Grossman. Approximate Program Synthesis. In *Workshop on Approximate Computing Across the Stack (WAX w/ PLDI)*, June 2015
79. Mark Wyse, Andre Baixo, Thierry Moreau, Bill Zorn, James Bornholt, Adrian Sampson, Luis Ceze, and Mark Oskin. REACT: A Framework for Rapid Exploration of Approximate Computing Techniques. In *Workshop on Approximate Computing Across the Stack (WAX w/ PLDI)*, June 2015
80. Thierry Moreau, Mark Wyse, Jacob Nelson, Adrian Sampson, Hadi Esmaeilzadeh, Luis Ceze, and Mark Oskin. SNNAP: Approximate Computing on Programmable SoCs via Neural Acceleration. In *International Symposium on High-Performance Computer Architecture (HPCA)*, February 2015
81. Brandon Lucia and Luis Ceze. Data Provenance Tracking for Concurrent Programs. In *International Symposium on Code Generation and Optimization (CGO)*, February 2015
82. Brandon Holt, Preston Briggs, Luis Ceze, and Mark Oskin. Alembic: Automatic Locality Extraction via Migration. In *SPLASH-OOPSLA*, October 2014
83. Tom Bergan, Dan Grossman, and Luis Ceze. Symbolic Execution of Multithreaded Programs from Arbitrary Program Contexts. In *SPLASH-OOPSLA*, October 2014
84. Renee St. Amant, Amir Yazdanbakhsh, Jongse Park, Bradley Thwaites, Hadi Esmaeilzadeh, Arjang Hassibi, Luis Ceze, and Doug Burger. General-Purpose Code Acceleration with Limited-Precision Analog Computation. In *International Symposium on Computer Architecture (ISCA)*, 2014. Selected for IEEE Micro Top Picks Honorable Mention 2015
85. Adrian Sampson, Pavel Panchekha, Todd Mytkowicz, Kathryn McKinley, Dan Grossman, and Luis Ceze. Expressing and Verifying Probabilistic Assertions. In *Conference on Programming Language Design and Implementation (PLDI)*, June 2014
86. Benjamin P. Wood, Luis Ceze, and Dan Grossman. Low-Level Detection of High-Level Data Races with LARD. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2014
87. Anthony Gutierrez, Michael Cieslak, Ronald G. Dreslinski, Luis Ceze, and Trevor Mudge. Mercury: An Integrated, 3D-Stacked Server Design for Increasing Physical Density of Key-Value Stores. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2014
88. Adrian Sampson, Jacob Nelson, Karin Strauss, and Luis Ceze. Approximate Storage in Solid-State Memories. In *International Symposium on Microarchitecture (MICRO)*, December 2013
89. Brandon Holt, Jacob Nelson, Brandon Myers, Preston Briggs, Luis Ceze, Simon Kahan, and Mark Oskin. Flat Combining Synchronized Global Data Structures. In *International Conference on PGAS Programming Models*, 2013
90. Katelin A Bailey, Peter Hornyack, Luis Ceze, Steven D. Gribble, and Henry M. Levy. Exploring Storage Class Memory with Key Value Stores. In *Workshop on Interactions of NVM/FLASH with Operating Systems and Workloads*, 2013
91. Adrian Sampson, Luis Ceze, and Dan Grossman. EnerJ, the Language of Good-Enough Computing. *IEEE Spectrum Feature Article*, October 2013

92. Tom Bergan, Luis Ceze, and Dan Grossman. Input-Covering Schedules for Multithreaded Programs. In *SPLASH-OOPSLA*, October 2013
93. Richard Muscat, Karin Strauss, Luis Ceze, and Georg Seelig. DNA-based Molecular Architecture with Spatially Localized Components. In *International Symposium on Computer Architecture (ISCA)*, June 2013
94. Nicholas Hunt, Tom Bergan, Luis Ceze, and Steven Gribble. DDOS: Taming Nondeterminism in Distributed Systems. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2013
95. Brandon Lucia and Luis Ceze. Cooperative Empirical Failure Avoidance for Multithreaded Programs. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2013
96. Hadi Esmaeilzadeh, Adrian Sampson, Luis Ceze, and Doug Burger. Neural Acceleration for General-Purpose Approximate Programs. In *International Symposium on Microarchitecture (MICRO)*, December 2012. Selected for IEEE Micro Top Picks 2012
97. Tom Bergan, Dan Grossman, and Luis Ceze. Input-Covering Schedules for Multithreaded Programs. In *Workshop on Determinism and Correctness in Parallel Programming w/ International Conference on Architectural Support for Programming Languages and Operating Systems (WoDet w/ ASPLOS)*, March 2013
98. Adrian Sampson, Calin Cascaval, Luis Ceze, Pablo Montesinos, and Dario Suarez Gracia. Automatic Discovery of Performance and Energy Pitfalls in HTML and CSS. In *International Symposium on Workload Characterization (IISWC)*, November 2012
99. Laura Effinger-Dean, Brandon Lucia, Luis Ceze, Dan Grossman, and Hans-J. Boehm. IFRit: Interference-Free Regions for Dynamic Data-Race Detection. In *SPLASH-OOPSLA*, October 2012
100. Hadi Esmaeilzadeh, Adrian Sampson, Luis Ceze, and Doug Burger. Towards Neural Acceleration for General-Purpose Approximate Computing. In *Workshop on Energy Efficient Design w/ International Symposium on Computer Architecture (WEED w/ ISCA)*, June 2012
101. Hadi Esmaeilzadeh, Adrian Sampson, Michael Ringenburg, Luis Ceze, Dan Grossman, and Doug Burger. Addressing Dark Silicon Challenges with Disciplined Approximate Computing. In *Dark Silicon Workshop w/ International Symposium on Computer Architecture (DaSi w/ ASPLOS)*, June 2012
102. Joseph Devietti, Benjamin Wood, Karin Strauss, Luis Ceze, Shaz Qadeer, and Dan Grossman. RADISH: Always-On Sound and Complete RAce Detection In Software and Hardware. In *International Symposium on Computer Architecture (ISCA)*, June 2012
103. Hadi Esmaeilzadeh, Adrian Sampson, Luis Ceze, and Doug Burger. Architecture Support for Disciplined Approximate Programming. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2012
104. Brandon Lucia and Luis Ceze. Automatic Empirical Failure Avoidance for Concurrent Software. In *Workshop on Determinism and Correctness in Parallel Programming w/ International Conference on Architectural Support for Programming Languages and Operating Systems (WoDet w/ ASPLOS)*, March 2012
105. Joseph Devietti, Luis Ceze, and Dan Grossman. The Case For Merging Execution- and Language-level Determinism with MELD. In *Workshop on Determinism and Correctness in Parallel Programming w/ International Conference on Architectural Support for Programming Languages and Operating Systems (WoDet w/ ASPLOS)*, March 2012
106. Nicholas Hunt, Brandon Lucia, and Luis Ceze. System Introspection with Hardware Watchmachines. In *Fun Ideas and Thoughts w/ Conference on Programming Language Design and Implementation (PLDI FIT)*, 2011
107. Benjamin Wood, Luis Ceze, and Dan Grossman. Data-Race Exceptions Have Benefits Beyond the Memory Model. In *Workshop on Memory System Performance and Correctness w/ Conference on Programming Language Design and Implementation (MSPC w/ PLDI)*, June 2011

108. Rodrigo Gonzalez-Alberquilla, Karin Strauss, Luis Pinuel, and Luis Ceze. Accelerating Data Race Detection with Minimal Hardware Support. In *EuroPar*, August 2011
109. Katelin Bailey, Luis Ceze, Steven D. Gribble, and Henry M. Levy. Operating System Implications of Fast, Cheap, Non-Volatile Memory. In *USENIX Hot Topics on Operating Systems (HotOS)*, May 2011
110. Laura Effinger-Dean, Alexander Jaffe, Thomas Moscibroda, Karin Strauss, and Luis Ceze. On the Impact of Memory Models on Software Reliability in Multiprocessors. In *Symposium on Principles of Distributed Computing (PODC)*., June 2011
111. Jacob Nelson, Brandon Myers, A.H. Hunter, Preston Briggs, Dan Grossman, Mark Oskin, Carl Ebeling, Simon Kahan, and Luis Ceze. Crunching Large Graphs with Commodity Processors. In *USENIX Hot Topics on Parallelism (HotPar)*, June 2011
112. Adrian Sampson, Werner Dietl, Emily Fortuna, Danushen Gnanapragasam, Luis Ceze, and Dan Grossman. EnerJ: Approximate Data Types for Safe and General Low-Power Computation. In *Conference on Programming Language Design and Implementation (PLDI)*, June 2011
113. Brandon Lucia, Benjamin Wood, and Luis Ceze. Isolating and Understanding Concurrency Errors Using Reconstructed Execution Fragments. In *Conference on Programming Language Design and Implementation (PLDI)*, June 2011
114. Joseph Devietti, Jacob Nelson, Tom Bergan, Luis Ceze, and Dan Grossman. RCDC: A Relaxed Consistency Deterministic Computer. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2011
115. Jacob Nelson, Adrian Sampson, and Luis Ceze. Dense Approximate Storage in Phase-Change Memory. In *Wild and Crazy Ideas w/ International Conference on Architectural Support for Programming Languages and Operating Systems (WACI w/ ASPLOS)*, March 2011
116. Tom Bergan, Joseph Devietti, Nicholas Hunt, and Luis Ceze. The Deterministic Execution Hammer: How Well Does it Actually Pound Nails? In *Workshop on Determinism and Correctness in Parallel Programming w/ International Conference on Architectural Support for Programming Languages and Operating Systems (WoDet w/ ASPLOS)*, March 2011
117. Owen Anderson, Emily Fortuna, Luis Ceze, and Susan Eggers. Checked Load: Architectural Support for JavaScript Type-Checking on Mobile Processors. In *International Symposium on High-Performance Computer Architecture (HPCA)*, February 2011
118. Nicholas Hunt, Paramjit Singh Sandhu, and Luis Ceze. Characterizing the Performance and Energy Efficiency of Lock-Free Data Structures. In *Workshop on Interaction between Compilers and Computer Architectures w/ International Symposium on High-Performance Computer Architecture (INTERACT w/ HPCA)*, February 2011
119. Emily Fortuna, Owen Anderson, Luis Ceze, and Susan Eggers. A Limit Study of JavaScript Parallelism. In *International Symposium on Workload Characterization (IISWC)*, December 2010
120. Tom Bergan, Nicholas Hunt, Luis Ceze, and Steve Gribble. Deterministic Process Groups in dOS. In *Symposium on Operating Systems Design and Implementation (OSDI)*, October 2010
121. Benjamin Wood, Adrian Sampson, Luis Ceze, and Dan Grossman. Composable Specifications for Structured Shared-Memory Communication. In *SPLASH-OOPSLA*, October 2010
122. Brandon Lucia, Luis Ceze, Karin Strauss, Shaz Qadeer, and Hans-J. Boehm. Conflict Exceptions: Providing Simple Concurrent Language Semantics with Precise Hardware Exceptions for Data Races. In *International Symposium on Computer Architecture (ISCA)*, June 2010
123. Brandon Lucia, Luis Ceze, and Karin Strauss. ColorSafe: Architectural Support for Debugging and Dynamically Avoiding Multi-variable Atomicity Violations. In *International Symposium on Computer Architecture (ISCA)*, June 2010
124. Brandon Lucia, Joseph Devietti, Tom Bergan, Luis Ceze, and Dan Grossman. Lock Prediction. In *USENIX Hot Topics on Parallelism (HotPar)*, June 2010

125. Tom Bergan, Owen Anderson, Joseph Devietti, Luis Ceze, and Dan Grossman. CoreDet: A Compiler and Runtime System for Deterministic Multithreaded Execution. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2010
126. Joseph Devietti, Brandon Lucia, Luis Ceze, and Mark Oskin. DMP: Deterministic Shared Memory Multiprocessing. *IEEE Micro Top Picks in Computer Architecture*, February 2010
127. Luis Ceze. *Encyclopedia of Parallel Computing, Editor: David Padua*, chapter Shared-Memory Multiprocessors. Springer, January 2010
128. Brandon Lucia and Luis Ceze. Finding Concurrency Bugs with Context-Aware Communication Graphs. In *International Symposium on Microarchitecture (MICRO)*, December 2009
129. Josep Torrellas, Luis Ceze, James Tuck, Calin Cascaval, Pablo Montesinos, Wonsun Ahn, and Milos Prvulovic. The bulk multicore architecture for improved programmability. *Communication of the ACM*, December 2009
130. Jacob Nelson and Luis Ceze. Concurrency Discovery for Very Large Windows of Execution. In *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures w/ International Symposium on Computer Architecture (PESPMA w/ ISCA)*, June 2009
131. Derek R. Hower, Pablo Montesinos, Luis Ceze, Mark D. Hill, and Josep Torrellas. Two Hardware-based Approaches for Deterministic Multiprocessor Replay. *Research Highlights, Communication of the ACM*, June 2009
132. Luis Ceze, Joseph Devietti, Brandon Lucia, and Shaz Qadeer. The Case for System Support for Concurrency Exceptions. In *USENIX Hot Topics on Parallelism (HotPar)*, June 2009
133. Joseph Devietti, Brandon Lucia, Luis Ceze, and Mark Oskin. DMP: Deterministic Shared Memory Multiprocessing. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2009. Selected for IEEE Micro Top Picks 2009
134. Andrew Putnam, Luis Ceze, and Bryna Hazelton. Self-Powered Processors. In *Wild and Crazy Ideas w/ International Conference on Architectural Support for Programming Languages and Operating Systems (WACI w/ ASPLOS)*, March 2009
135. Brandon Lucia, Joseph Devietti, Karin Strauss, and Luis Ceze. Atom-aid: Detecting and surviving atomicity violations. *IEEE Micro Top Picks in Computer Architecture*, February 2009
136. James Tuck, Wonsun Ahn, Luis Ceze, Josep Torrellas, and Luis Ceze. Softsig: Software-exposed hardware signatures for memory disambiguation. *IEEE Micro Top Picks in Computer Architecture*, February 2009
137. Luis Ceze, Christoph von Praun, Calin Cascaval, Pablo Montesinos, and Josep Torrellas. Programming and Debugging Shared Memory Programs with Data Coloring. In *Workshop on Compilers for Parallel Computing (CPC)*, January 2009
138. Brandon Lucia, Joseph Devietti, Karin Strauss, and Luis Ceze. Atom-Aid: Detecting and Surviving Atomicity Violations. In *International Symposium on Computer Architecture (ISCA)*, June 2008. Selected for IEEE Micro Top Picks 2008
139. Pablo Montesinos, Luis Ceze, and Josep Torrellas. DeLorean: Recording and Deterministically Replaying Shared-Memory Multiprocessor Execution Efficiently. In *International Symposium on Computer Architecture (ISCA)*, June 2008
140. Joseph Devietti, Brandon Lucia, Mark Oskin, and Luis Ceze. Explicitly Parallel Programming with Shared-Memory is Insane: At Least Make it Deterministic! In *Workshop on Software and Hardware Challenges of Manycore Platforms w/ International Symposium on Computer Architecture (SHCMP w/ ISCA)*, June 2008
141. James Tuck, Wonsun Ahn, Luis Ceze, and Josep Torrellas. SoftSig: Software-Exposed Hardware Signatures for Memory Disambiguation. In *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2008. Selected for IEEE Micro Top Picks 2008

142. Luis Ceze, Christoph von Praun, Calin Cascaval, Pablo Montesinos, and Josep Torrellas. Concurrency Control with Data Coloring. In *Workshop on Memory Systems Performance and Correctness w/ International Conference on Architectural Support for Programming Languages and Operating Systems (MSPC w/ ASPLOS)*, March 2008
143. Luis Ceze, James Tuck, Pablo Montesinos, and Josep Torrellas. BulkSC: Bulk Enforcement of Sequential Consistency. In *International Symposium on Computer Architecture (ISCA)*, June 2007
144. Christoph von Praun, Luis Ceze, and Calin Cascaval. Implicit Parallelism with Ordered Transactions. In *Principles and Practice of Parallel Programming (PPoPP)*, February 2007
145. Luis Ceze, Pablo Montesinos, Christoph von Praun, and Josep Torrellas. Colorama: Architectural Support for Data-Centric Synchronization. In *International Symposium on High-Performance Computer Architecture (HPCA)*, February 2007
146. James Tuck, Luis Ceze, and Josep Torrellas. Scalable Cache Miss Handling for High Memory Level Parallelism. In *International Symposium on Microarchitecture (MICRO)*, December 2006
147. Luis Ceze, James Tuck, Calin Cascaval, and Josep Torrellas. Bulk Disambiguation of Speculative Threads in Multiprocessors. In *International Symposium on Computer Architecture (ISCA)*, June 2006
148. Wei Liu, James Tuck, Luis Ceze, Wonsun Ahn, Karin Strauss, Jose Renau, and Josep Torrellas. POSH: A TLS Compiler that Exploits Program Structure. In *Principles and Practice of Parallel Programming (PPoPP)*, February 2006
149. Luis Ceze, Karin Strauss, James Tuck, Jose Renau, and Josep Torrellas. Using Checkpoint-Assisted Value Prediction to Hide L2 Misses. *ACM Transactions on Architecture and Code Optimization (TACO)*, January 2009
150. Luis Ceze, James Tuck, and Josep Torrellas. Are We Ready for High Memory-Level Parallelism? In *Workshop on Memory Performance Issues w/ International Symposium on High-Performance Computer Architecture (WMPI w/HPCA)*, February 2006. Also appears in SIGMICRO Newsletter selection from WMPI-2006
151. Jose Renau, Karin Strauss, Luis Ceze, Smruti Sarangi, James Tuck, Wei Liu, and Josep Torrellas. Energy-Efficient Thread-Level Speculation on a CMP. *IEEE Micro Top Picks in Computer Architecture*, January 2006
152. Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. Thread-Level Speculation on a CMP Can Be Energy Efficient. In *International Conference on Supercomputing (ICS)*, June 2005. Selected for IEEE Micro Top Picks 2005
153. Jose Renau, James Tuck, Wei Liu, Luis Ceze, Karin Strauss, and Josep Torrellas. Tasking with Out-of-Order Spawn in TLS Chip Multiprocessors: Microarchitecture and Compilation. In *International Conference on Supercomputing (ICS)*, June 2005. Selected for IEEE Micro Top Picks 2005
154. Luis Ceze, Karin Strauss, James Tuck, Jose Renau, and Josep Torrellas. CAVA: Hiding L2 Misses with Checkpoint-Assisted Value Prediction. *IEEE Computer Architecture Letters (CAL)*, December 2004
155. George Almasi, Ralph Bellofatto, Jose Brunheroto, Calin Cascaval, Jose G. Castanos, Luis Ceze, et al. An Overview Of The Blue Gene/L System Software Organization. *International Conference on Parallel and Distributed Computing (Euro-Par)*, October 2003
156. Luis Ceze, Karin Strauss, et al. Full Circle: Simulating Linux Clusters on Linux Clusters. *LCI International Conference on Linux Clusters (CWCE)*, March 2003. Selected as one of the top 3 papers in the conference
157. N. R. Adiga et al. An Overview of the Blue Gene/L Supercomputer. In *IEEE Supercomputing (SC)*, November 2002
158. G. Almasi et al. Blue Gene/L, a system-on-a-chip. In *IEEE International Conference on Cluster Computing (CC)*, December 2002
159. Calin Cascaval, Jose G. Castanos, Luis Ceze, Monty Denneau, Manish Gupta, Derek Lieber, Jose E. Moreira, Karin Strauss, and Henry S. Warren Jr. Evaluation of a Multithreaded Architecture for Cellular Computing. In *International Symposium on High-Performance Computer Architecture (HPCA)*, February 2002

160. G. Almasi et al. Cellular Supercomputing with System-on-a-Chip. In *International Solid State Circuits Conference (ISSCC)*, February 2002
161. I. Stiubiener, L.H. Ceze, K. Strauss, C.B. Margi, R.M. Silveira, and W.V. Ruggiero. An environment for easy cross synchronization of multimedia web based material. In *Frontiers in Education*, October 2000

PATENTS ISSUED

USPTO search link: `https://bit.ly/3PmZ5GK`

1. Matthew Welsh, Jason Knight, Jared Roesch, Thierry Moreau, Adelbert Chang, Tianqi Chen, Luis Ceze, An Wang, Michal Piszczek, Andrew McHarg, Fletcher Haynes, "*Optimizing machine learning models with a device farm*", February 2021.
2. Matthew Welsh, Jason Knight, Jared Roesch, Thierry Moreau, Adelbert Chang, Tianqi Chen, Luis Ceze, An Wang, Michal Piszczek, Andrew McHarg, Fletcher Haynes, "*Optimizing machine learning models*", February 2021.
3. Luis Ceze, Georg Seelig, "*Integrated system for nucleic acid-based storage and retrieval of digital data using keys*", February 2018.
4. Karin Strauss, Siena Dumas Ang, Luis Ceze, Yuan-Jyue Chen, Hsing-Yeh Parker, Bichlien Nguyen, Robert Carlson, "*Polynucleotide sequencer tuned to artificial polynucleotides*", May 2017.
5. Yuan-Jyue Chen, Luis Ceze, Sergey Yekhanin, Siena Dumas Ang, Karin Strauss, "*Primer and payload design for retrieval of stored polynucleotides*", February 2017.
6. Yuan-Jyue Chen, Karin Strauss, Luis Ceze, Siena Dumas Ang, Sergey Yekhanin, "*Generating pluralities of primer and payload designs for retrieval of stored nucleotides*", Feburary 2017.
7. Yuan-Jyue Chen, Karin Strauss, Luis Ceze, Lee Organick, "*Random access of data encoded by polynucleotides*", March 2017.
8. Yuan-Jyue Chen, Karin Strauss, Luis Ceze, Lee Organick, Randolph Lopez, Georg Seelig, "*Modifications to polynucleotides for sequencing*", February 2017.
9. Luis Ceze, Gheorghe C. Cascaval, Mohammad H. Reshadi, "*Reducing web browsing overheads with external code certification*", November 2017.
10. Karin Strauss, Luis Ceze, Henrique S. Malvar, Qing Guo, "*Dynamic approximate storage for custom applications*", October 2017.
11. Karin Strauss, Luis Ceze, Henrique S. Malvar, Qing Guo, "*Data encoding on single-level and variable multi-level cell storage*", July 2017.
12. Matthias A. Blumrich, Luis Ceze, Dong Chen, Alan Gara, Philip Heidelberger, Martin Ohmacht, Burkhard Steinmacher-Burow, Xiaotong Zhuang, "*Cache as point of coherence in multiprocessor system*", November 2016.
13. Daniel Ahn, Luis Ceze, Dong Chen, Alan Gara, Philip Heidelberger, Martin Ohmacht, "*Multiprocessor system with multiple concurrent modes of execution*", November 2016.
14. Karin Strauss, Douglas Burger, Luis Ceze, Adrian Sampson, "*Approximate multi-level cell memory operations*", August 2016.
15. Susan Eggers, Luis Ceze, Emily Fortuna, Owen Anderson, "*Systems and methods for hardware-assisted type checking*", May 2016.
16. Luis Ceze, Calin Cascaval, Bin Wang, Michael P. Maha, Chettan S. Dillon, Wendell Ruotsi, Vikram Mandyam, "*Memoizing web-browsing computation with DOM-based isomorphism*", October 2015.
17. Luis Ceze, Thomas Bergan, Joseph Devietti, Daniel Grossman, Jacob Nelson, "*Systems and methods for providing deterministic execution*", September 2015.
18. Luis Ceze and Brandon Lucia, "*Systems and methods for finding concurrency errors*", August 2014.
19. Luis Ceze, Mohammad Reshadi, Thomas Sartorius, "*Hardware support for hashtables in dynamic languages*", June 2015.

20. Karin Strauss, Adrian Sampson, Luis Ceze, "*Priority-assignment interface to enhance approximate computing*", April 2015.
21. Karin Strauss, Adrian Sampson, Luis Ceze, Doug Burger,"*Approximate multi-level cell memory operations*", March 2013.
22. Luis Ceze and Brandon Lucia, "*Systems and methods for finding concurrency errors*", September 2014.
23. Daniel Ahn, Luis Ceze, et al., "*Reader set encoding for directory of shared cache memory in multiprocessor system*", June 2014.
24. Luis Ceze, Peter Godman and Mark Oskin, "*Computer-implemented system and method for providing software fault tolerance*", June 2014.
25. Luis Ceze, Mark Oskin, Joseph Devietti and Brandon Lucia, "*Critical path deterministic execution of multithreaded applications in a transactional memory system*", May 2014.
26. Luis Ceze and Mark Oskin, "*Deterministic serialization in a transactional memory system based on thread creation order*", April 2014.
27. Daniel Ahn, Luis Ceze et al., "*Multiprocessor system with multiple concurrent modes of execution*", December 2013.
28. Luis Ceze, Peter Godman and Mark Osking, "*Enhanced reliability using deterministic multiprocessing-based synchronized replication*", May 2013.
29. Christoph von Praun and Luis Ceze, "*Method and apparatus to trigger synchronization and validation actions upon memory access* ", December 2012.

TEACHING

UW course evaluations are in a scale of 0 to 5.0.

- Spring 2020, CSE599X: Molecular Information Systems, CSE, UW. *Course eval: 4.9*
- Winter 2020, CSE548P: Computer Systems Architecture (PMP), CSE, UW. *Course eval: 4.8*
- Spring 2019, CSE548: Computer Systems Architecture, CSE, UW. *Course eval: 4.8*
- Winter 2019, CSE351: The Hardware/Software Interface, CSE, UW. *Course eval: 4.5*
- Spring 2018, CSE599S: HW/SW Co-Design for Machine Learning, CSE, UW. *Course eval: 4.4*
- Autumn 2017, CSE548P: Computer Systems Architecture (PMP), CSE, UW. *Course eval: 4.8*
- Spring 2017, CSE548: Computer Systems Architecture, CSE, UW. *Course eval: 4.9*
- Winter 2017, CSE351: The Hardware/Software Interface, CSE, UW. *Course eval: 5.0*
- Autumn 2015, CSE548P: Computer Systems Architecture (PMP), CSE, UW. *Course eval: 4.8*
- Winter 2015, CSE351: The Hardware/Software Interface, CSE, UW. *Course eval: 5.0*
- Autumn 2014, CSE548: Computer Systems Architecture, CSE, UW. *Course eval: 4.9*
- Summer 2014, The Hardware/Software Interface, Coursera.
- Spring 2013, The Hardware/Software Interface, Coursera.
- Spring 2013, CSE351: The Hardware/Software Interface, CSE, UW. *Course eval: 5.0*
- Autumn 2012, CSE548P: Computer Systems Architecture (PMP), CSE, UW. *Course eval: 4.7*
- Autumn 2011, CSE351: The Hardware/Software Interface, CSE, UW. *Course eval: 4.9*
- Spring 2011, CSE351: The Hardware/Software Interface, CSE, UW. *Course eval: 4.9*
- Winter 2011, CSE548P: Computer Systems Architecture (PMP), CSE, UW. *Course eval: 4.6*
- Spring 2010, CSE378: Machine Organization and Assembly Language, CSE, UW. *Course eval: 4.9*
- Winter 2010, CSE548: Computer Systems Architecture, CSE, UW. *Course eval: 4.7*
- Spring 2009, CSE548P: Computer Systems Architecture (PMP), CSE, UW. *Course eval: 4.2*

- ◇ Winter 2009, CSE378: Machine Organization and Assembly Language, CSE, UW. *Course eval: 4.8*
- ◇ Spring 2008, CSE599Q: Topics in Multiprocessor Programmability, CSE, UW. *Course eval: 4.4*
- ◇ Winter 2008, CSE548: Computer Systems Architecture, CSE, UW. *Course eval: 4.5*
- ◇ Winter 2008, CSE590P: Programming Systems Seminar (w/ Dan Grossman), CSE, UW.
- ◇ Fall 2007, CSE378: Machine Organization and Assembly Language, CSE, UW. *Course eval: 4.5*
- ◇ Spring 2005, CS533: Parallel Computer Architecture (TA), CS, UIUC.
- ◇ 2000, Cisco Networking Academy, University of São Paulo.

SELECTED INVITED TALKS

Keynote at Usenix FAST'21 on DNA Data Storage, Feb 2021.

"DNA Data Storage and Near-Molecule Processing for the Yottabyte Era", CIDR 2019 Keynote, January 2019; Huawei STW, May 2018.

"Approximate Computing from Language to Hardware and Beyond", ERAD-SP Keynote, Brazil, April 2018.

"Borrowing from Nature to Build Better Computers", Scale Keynote, August 2017; UW CoE Lecture Series, October 2017; Future Forum Keynote, October 2017; International Conference in Rebooting Computing Keynote, November 2017.

"A DNA-based Archival Storage System", SNIA Data Storage Innovation Conference Keynote, June 2016; Samsung, July 2016; Library of Congress, September 2016; Industry-Academia Partnership Workshop, Mar 2017.

"Silicon Meets Biotech: Building Better Computers by Borrowing from Nature", ASPLOS WACI, May 2016; Snowbird, July 2016.

"Approximate Overview of Approximate Computing", Schloss Dagstuhl, Workshop on Approximate Computing, November 2015.

"Approximate Computing Across the System Stack", Intel Corp., April 2015.

"Imperfection is Beautiful and Efficient: Approximate Computing from Language to Hardware and Beyond", NII Japan, October 2015; Kyushu University, October 2015; Qumulo Inc., August 2015; TU Dresden, May 2015; PNNL Signature Discovery Lectures, Mar 2015; UGrad Research Symposium, Nov 2014.

"Imperfection is Beautiful and Efficient: Approximate computing can enable a new wave of systems and substrates", DARPA MTO off-site meeting, Oct 2014.

"In-network processing and NVRAM in Grappa", Schloss Dagstuhl, Workshop on Systems and Algorithms for Large-scale Graph Analytics, November 2014.

"A Crash Course on Cache Coherence and Memory Consistency Models", Apple Computer, September 2014.

"Disciplined Approximate Computing: From Language to Hardware and Beyond", Microsoft Research Cambridge, September 2013; University of Edingburgh, Scotland, September 2013; ETH Zurich, October 2013; Ghent University, October 2013; University of Cambridge, October 2013; Samsung Korea, November 2013; Seoul National University, November 2013; Sungkyunkwan University, November 2013; University of Uppsala, November 2013; Chalmers University, November 2013; Intel Barcelona, December 2013; Distinguished Lecture at INESC-ID, Lisbon Portugal, Mar 2014; University of Wisconsin, April 2014; Yale University, December 2014.

"Concurrency, Approximation, Graphs and DNA in Computer Architecture Research", University of Cambridge, UK, August 2013.

"Disciplined Approximate Computing: From Language to Hardware", NANOENERGY 2013, Perugia Italy, July 2013; Intel Labs, Hillsboro OR, June 2013; IBM Research, May 2013; Google, April 2013; Oracle Labs, March 2013; EPFL, January 2013; NIAC w/ HiPEAC, January 2013; INRIA Saclay, November 2012; University of Michigan, Ann Arbor, November 2012; IBM Research, May 2013.

"Hot/Emerging Topics in Computer Architecture", CRA-W Architecture Summer School, August 2012.

"Safe and General Energy-Aware Programming with Disciplined Approximation", University of California at Santa Barbara, June 2012; Pacific Northwest National Lab, May 2012; University of Sao Paulo, Brazil. April 2012; Microsoft Research, November 2011; AMD RadLabs, November 2011; Qualcomm, August 2011; Energy-Aware Computing Workshop, University of Bristol, July 2011.

"Challenges of Disruptive Systems Research", MSR Faculty Fellows Panel, May 2011.

"Determinism and Fail-Stop Races for Sane Multiprocessing", Northwest C++ Users Group, January 2011; University of Cambridge, November 2013.

"A Case for Concurrency Exceptions: Fail-stop Behavior for Sane Multiprocessing", Schloss Dagstuhl, Workshop on Memory Models, January 2011.

"Some Recent Fun with JavaScript", Microsoft Research, December 2010.

"Determinism and Fail-Stop Races for Sane Multiprocessing", Intel Santa Clara, December 2010; Carnegie Mellon University, ASPLOS PC Workshop, October 2010.

"Sequential Execution of Parallel Programs", Keynote Address, ISCA Workshop on Parallel Execution of Sequential Programs, France, June 2010.

"Deterministic Shared Memory Multiprocessing", SIAM Conference on Parallel Processing for Scientific Computing, February 2010.

"Threads Should Not Play Dice: Exploring Determinism (and Nondeterminism) in Multithreaded Applications", Qualcomm, February 2010.

"Lecture Series in Multiprocessor Programmability", National Institute of Informatics, Japan, September 2009.

"Threads Should Not Play Dice: Determinism and Bug Avoidance for Multithreaded Applications", IBM Research Yorktown, July 2009; University of Michigan, June 2009; Cornell University, April 2009.

"The Case For Deterministic Shared Memory Multiprocessing and Its Impact On Programmability", IBM Research Yorktown, September 2008.

"Making Multiprocessors Less Scary with Bulk Operations", MSR Asia, June 2008; IBM China Research Lab, June 2008.

"The Case for A Fully Deterministic Multiprocessor Architecture", MSR Redmond, October 2007.

"Multiprocessor Architectures for Programmability", University of Washington, MSR Redmond, Intel Research Pittsburgh, Carnegie Mellon University, IBM Research Yorktown, University of Michigan, Massachusetts Institute of Technology, Caltech, Columbia University, 2007.

ACADEMIC SERVICE

ASPLOS 2020 PC co-chair.

ASPLOS 2019, PC member.

ASPLOS 2018, PC member, WACI co-chair.

Member of DARPA MEC Study Group, 2017-2019.

Member of DARPA ISAT Study Group, 2013-2019.

SIGARCH Visioning Committee Member.

ISCA 2017, PC Member.

IEEE Micro Top Picks 2017, Program Committee Member.

Architecture 2030 (w/ ISCA 2016), Co-organizer.

ISCA 2016, PC Member.

DARPA ISAT Workshop on Future of Storage, Co-chair, May 2016.

Workshop on Approximate Computing Across the Stack (WAX w/ PLDI) 2015, Co-chair.

DARPA ISAT Workshop on Silicon Meets Biotech, Co-chair, Mar 2015.

SOSP 2015, PC Member.

IEEE Micro Special Edition on Alternative Computing 2015, Invited co-editor.

IEEE Computer Architecture Letters Associate Editor, 2014-present.

ISCA 2015, PC Member.

IEEE Micro Top Picks 2015, PC Co-Chair.

Transactions on Parallel Computing, Editorial Board member, 2013-present.

MICRO 2014, PC Member.

Invited Panelist at ACM TAPIA Conference 2014.

DARPA ISAT Workshops on Survivalist Computing, Co-chair, August 2014 and November 2014.

DARPA ISAT Workshop on Approximate Computing, Co-chair, Feb 2014.

Workshop on Approximate Computing Across the Stack (WACAS w/ ASPLOS) 2014, Co-chair.

ASPLOS 2014, WACI co-chair.

Invited instructor at ACACES Summer School, July 2013.

Invited participant of DARPA ISAT Workshop on Resilience, Mar 2013.

OSDI 2014, External Review Committee Member.

ASPLOS 2014, PC Member.

USENIX HotPar 2013, PC Member.

PACT Student Research Competition 2013, Committee Member.

Member of the USENIX HotPar Steering Committee, 2012-present.

Member of Editorial Board for ACM Transactions on Parallel Computing.

Invited participant of NSF ACAR (Advancing Computer Architecture Research), and DARPA ISAT on Advancing Computer Systems.

IEEE Micro Top Picks 2013, Program Committee Member.

MICRO 2012, External Review Committee.

USENIX HotPar 2012, Program Co-Chair.

SBAC-PAD 2012, Architecture Track, Program Committee Member.

HPPC 2011 (held w/MICRO), Program Committee Member.

Workshop on Energy-efficient Computing for a Sustainable World (held w/ MICRO), Co-organizer.

WoDet 2012, Steering Committee and Program Committee Member.

ISCA 2012, Industrial Liaison Co-Chair.

ASPLOS 2012, External Review Committee Member.

PLDI 2012, External Review Committee Member.

PPoPP 2012, Program Committee Member.

SBAC-PAD 2011, Architecture Track, Program Committee Member.

MICRO 2011, Program Committee Member.

MSPC 2011, Program Committee Member.

PLDI 2011, External Review Committee Member.

WoDet (held w/ ASPLOS) 2011, Organizer.

ASPLOS 2011, Program Committee Member.

MICRO 2010, Program Committee Member.

Workshop on Deterministic Multiprocessing and Parallel Programming (WoDet) 2009, Organizer.

ASPLOS 2010, Program Committee Member.

ISCA 2009, Workshops/Tutorials co-chair.

PESPMA 2009 (held w/ ISCA) , Program Committee Member.

ASPLOS 2009, Program Committee Member.

UW-MSR Summer Institute 2008, co-organizer.

IISWC 2008, Program Committee Member.

ASPLOS-WACI 2008, Program Committee Member.

ISCA 2008, Program Committee Member.

ASPLOS 2008, Local Arrangements co-chair.

Maintainer of SESC, a cycle-accurate multiprocessor simulator (sesc.sourceforge.net).

Volunteer Member of Technical Staff, Networld+Interop, Las Vegas (2001).

Cisco Certified Academy Instructor (2000).

Cisco Networking Academy, Cisco Certified Network Associate (1999 – 2000).

Helped organize the Computer Architecture Reading Group at the CS Department, UIUC.

Paper Reviewer for MICRO, ISCA, HPCA, P=ac2, PPoPP, PLDI, LCPC, CAL, TACO, Usenix, TOPLAS, and Journal of Parallel Computing.

Member of ACM and IEEE. Associated member of HiPEAC.

CURRENT GRADUATE STUDENTS

Zihao Ye (MLsys)

Chien-Yu Lin (MLsys)

Lee Organick (DNA nanotech)

Ashley Stephenson (closed-loop molecular design)

Gus Smith (PL+architecture)

GRADUATED STUDENTS

Luis Vega, PhD., 2022 (first job: startup co-founder)

Max Willsey, PhD., 2021 (first job: Postdoc at University of Washington)

Amrita Mazumbar, PhD., 2021 (first job: NVIDIA)

Meghan Cowan, PhD., 2021 (first job: Microsoft Research)

Eddie Yan, PhD., 2021 (first job: NVIDIA)

Katie Doroschak, PhD., 2020 (first job: Computational Biologist at Adaptive Biotechnologies)

Callie Bee, PhD., 2020 (first job: Researcher at University of Washington)

Ming Liu, PhD., 2020 (first job: Assistant Professor at University of Wisconsin)

Liang Luo, PhD., 2020 (first job: Research Scientist at Facebook)

Amrita Mazumdar, PhD., 2020 (first job: Entrepreneurship post-doc at UW)

Tianqi Chen, PhD., 2019 (first job: Co-founder at OctoML, faculty at CMU)

James Bornholt, PhD., 2019 (first job: Assistant Professor at UT Austin)

Vincent Lee, PhD., 2019 (first job: Research Scientist at Facebook)

Thierry Moreau, PhD., 2018 (first job: post-doc at UW-CSE, co-founder at OctoML)

Brandon Holt, PhD., 2016 (first job: Apple)

Adrian Sampson, PhD., 2015 (first job: Assistant Professor at Cornell University)

Jacob Nelson, PhD., 2014 (first job: post-doc at UW-CSE, now at Microsoft Research)

Benjamin Wood, PnD., 2014 (first job: Wellesley College)

Thomas Bergan, PhD., 2014 (first job: Google)

Mike Ringenburg, PhD., 2014 (first job: Architect at Cray Inc.)

Hadi Esmaeilzadeh, PhD., 2013 (first job: Assistant Professor at GeorgiaTech)

Brandon Lucia, PhD., 2013. (first job: Researcher at Microsoft Research, now Assistant Professor at Carnegie Mellon University)

Joseph Devietti, PhD., 2012. (first job: Assistant Professor at the University of Pennsylvania).

Katelin Bailey, MS, 2015. (first job: Microsoft)

Andre Baixo, MS, 2015. (first job: ARM)

Nick Hunt, MS, 2012.

Emily Fortuna, MS, 2011. (first job: Google).

Owen Anderson, MS, 2010. (first job: Apple).

Nicholas Murphy, MS, 2009. (first job: grad student at Harvard).

Cherie Cheung, MS, 2008. (first job: financial institution in Hong Kong).

EXTERNAL ACTIVITIES

- Consultant for Microsoft, June 2012-present.
- Consultant for Qualcomm, August 2010-August 2011.
- Co-founder, Corensic (former PetraVM, start-up company out of UW-CSE), October 2008-January 2012.

FUNDING

- $5,000k, Microsoft. PI: Luis Ceze. "*Molecular Information Systems*".
- July 2019, $3,000k, DARPA. PI: Luis Ceze, Michael Taylor, Zach Tatlock. "*BlurWare: Realtime Machine Learning HW/SW Co-design*".
- December 2018, $750k, Huawei, Xilinx, Oracle, Intel, Apple. PI: Luis Ceze. "*Towards Automated End-to-End Compilation and Optimization for Deep Learning*".
- July 2018, $9M, DARPA. PIs: Michael Taylor, Luis Ceze, Mark Oskin, Adrian Sampson (Cornell), Zhiru Zhang, Christopher Batten . "*HammerBlade: Continuous Synthesis of Polymorphic Hardware/Software*".
- December 2018, $750k, Huawei, Xilinx, Oracle, Intel, Apple. PI: Luis Ceze. "*Towards Automated End-to-End Compilation and Optimization for Deep Learning*".
- January 2018, $6,340k, DARPA. PI: Luis Ceze. "*DNA Data Storage with Integrated Information Storage*".
- January 2018, $1,150k, DARPA/SRC. PI: Luis Ceze. "*CRISP – Center for Research on Intelligent Storage and Processing-in-memory*".
- June 2017, $2,000k, NSF. PIs: Ras Bodik, Alvin Cheung, Emina Torlak and Luis Ceze. "*ARION: Taming Heterogeneity with DSLs, Approximation, and Synthesis*".
- June 2017, $900k, NSF. PIs: Magda Balazinska and Luis Ceze. "*A Visual Cloud for Virtual Reality Applications*".
- May 2017, $100k, Oracle. PI: Luis Ceze. "*Inferring and Generate Code for Reconfigurable Hardware Fabrics*".

- July 2016, $1,200k, Microsoft. PI: Luis Ceze. "*Long-term Data Archival in DNA*".
- January 2016, $65k cash, Microsoft. PI: Luis Ceze. "*Long-term Data Archival*".
- October 2015, $8M, DARPA. PIs: Ras Bodik, Dan Grossman, Luis Ceze, Alvin Cheung, Michael Ernst, Zachary Tatlock, and Emina Torlak, Xi Wang. "*BRASS: A Picture is Worth a Billion Bits: Adaptive Visualization of Big Data*".
- October 2015, $100k, Oracle. PIs: Luis Ceze and Mark Oskin. "*Near-Flash Processing*".
- September 2015, $929k, Microsoft. PI: Luis Ceze. "*Dense Archival Storage*".
- July 2015, $2,400k, NSF. PIs: Luis Ceze, Dan Grossman, Emina Torlak and Mark Oskin. "*Approximate Computing Across the System Stack*".
- October 2014, $400k, DARPA. PIs: Luis Ceze and Mark Oskin. "*Understanding the Potential of Approximate Computing*".
- October 2014, $60k cash, Google. Sole PI. "*Approximate Wireless Communication*".
- October 2014, $50k cash, Microsoft. Sole PI. "*End-to-End Approximate Computing*".
- September 2014, $45k cash, NetApp Faculty Fellowship Award. PIs: Luis Ceze and Hank Levy. "*Leveraging Non-Volatile Memories with Versioned Key-Value Stores*".
- May 2014, $950k, NSF CCF. PIs: Georg Seelig and Luis Ceze. "*DNA-based Molecular Architecture with Spatially Localized Components*".
- September 2013, $45k cash, NetApp Faculty Fellowship Award. PIs: Luis Ceze and Mark Oskin. "*Towards an Architecture for Large-Scale and Irregular In-Memory Analytics*".
- August 2013, $750k, NSF CCF. PIs: Mark Oskin, Luis Ceze and Simon Kahan. "*Scalable Parallelism for Irregular and Graph Applications*".
- August 2013, $390k, ARO. PIs: Mark Oskin and Luis Ceze. "*Disciplined Approximate Computing for Energy Efficiency and Resilience*".
- August 2013, $70k cash, Oracle. PIs: Luis Ceze and Mark Oskin. "*GraphBench: A Benchmark Suite for Graph Analysis*"
- July 2013, $50k cash, Microsoft. Sole PI. "*Language and Hardware Support for Neural Acceleration*"
- March 2013, $1.78M. PIs: Luis Ceze and Dan Grossman, part of The Center for Future Architectures Research (C-FAR), led by the University of Michigan. Semiconductor Research Corporation and DARPA.
- February 2013, $311k, Intel. PIs: Luis Ceze, Steve Gribble, Hank Levy. "*New Operating System Abstractions and Applications for Non-Volatile Main Memory Systems* "
- November 2012, $50k cash, Microsoft. Sole PI. "*Neural Networks as Approximate Accelerators*"
- October 2012, $150k, PNNL. PIs: Luis Ceze, Mark Oskin and Dan Grossman. "*Large-Scale Graph Processing with Commodity Processors*"
- September 2012, $300k, NSF CCF. PIs: Luis Ceze and Dan Grossman. "*Disciplined Approximate Programming for Energy-Efficient Computing*".
- July 2012, $60k cash, Google. PIs: Luis Ceze and Hank Levy. "*Leveraging Non-Volatile Memories with Versioned Key-Value Stores*"
- February 2012, $40k cash, Microsoft. Sole PI. "*Approximate Accelerators*"
- October 2011, $300k, PNNL. PIs: Luis Ceze and Dan Grossman. "*Large-Scale Graph Processing with Commodity Processors*"
- June 2011, $57k cash, Google. Sole PI. "*Data Types for Energy-Aware Programming*"
- March 2011, $40k cash, Microsoft. Sole PI. "*Architecture Support for Energy-Aware Programming*"
- March 2011, $16k, REU, NSF CCF. Sole PI.
- August 2011, $900k, NSF CCF. PIs: Luis Ceze and Dan Grossman. "*A Code-Centric Approach to Specifying, Checking, and Discovering Shared-Memory Communication*".

- October 2010, $256k, PNNL. PIs: Luis Ceze and Dan Grossman. "*Large-Scale Graph Processing with Commodity Processors*"
- October 2010, $50k, Qualcomm. Sole PI. "*Improving Energy Efficiency of Dynamic Languages in Mobile Devices*"
- August 2010, $500k, NSF CCF. PIs: Luis Ceze and Susan Eggers. "*Precise Concurrency Exceptions: Architecture Support, Semantics and System Implications*".
- June 2010, $35k, UW Royalty Research Fund. Sole PI. "*Exploring Code-Centric Communication-Graphs for Software Debugging*".
- May 2010, $16k, REU, NSF CAREER. Sole PI.
- April 2010, $140k, Intel. PIs: Luis Ceze, Hank Levy and Steve Gribble. "*New Operating System Abstractions for Non-Volatile Main Memory Systems*"
- February 2010, $50k, Sloan Research Fellowship. Sole PI.
- July 2009, $30k, NSF Support for the First Workshop on Deterministic Multiprocessing (WoDet). Sole PI.
- June 2009, $200k cash, Microsoft New Faculty Fellowship. Sole PI.
- May 2009, $30k cash, Intel. Sole PI. "*A Recommendation Approach to Parallelizing Sequential Code*".
- May 2009, $12k, REU for NSF CAREER. Sole PI.
- April 2009, $80k cash, Google. PIs: Luis Ceze and Susan Eggers. "*Using Programmable Memory Semantics for Concurrency Exceptions and Debugging on Multi-cores*".
- March 2009, $450k + $81k supplement, NSF CAREER. Sole PI. "*CAREER: Deterministic Shared Memory Multiprocessing: Vision, Architecture and Impact on Programmability*".
- March 2008, $17K cash + $8K equipment, Intel. Sole PI. "*Research and Education on Finding and Preventing Concurrency Bugs*".
- March 2008, $35K cash, Microsoft. PIs: Luis Ceze and Steve Gribble. "*Understanding the Complexity of Virtual Machine Consolidation*".
- January 2008, $25K cash, Microsoft. Sole PI. "*Detecting and Surviving Concurrency Bugs*".
- September 2007, $210K, NSF CSR Subcontract. Sole PI. "*Novel Programming Models and Architectures to Simplify Parallel Programming*".