A Low-Noise, GaAs/AlGaAs, Microwave Frequency-Synthesizer IC

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Abstract— We have developed a GaAs/AlGaAs frequency-synthesizer IC with a 5.5 GHz feedback divider, a 2 GHz reference divider, a 500 MHz phase–frequency detector, 1 ns charge-pump pulses, and a gain-normalized charge-pump output with ±8 mA peak current and an 18 pA/√Hz noise floor. The feedback divider allows continuously selectable divide ratios from 12 to 16383, and supports dual-modulus pulse-swallowing fractional synthesis with single-bit control. The reference divider allows continuously selectable divide ratios from 1 to 4095; an optional divide-by-four/five input prescaler extends the divide ratios to 20475. The chip consumes 1 W from +5 V and –5.2 V supplies.

I. Introduction

Phase-locked loops (PLLs) are used extensively in modern communication systems, to generate sinusoids for signaling, and to extract information from received signals. Phase noise, power consumption, and frequency resolution are the primary measures of loop performance: Designers of satellite communication systems, for example, carefully optimize their PLLs to minimize transmitter and receiver phase noise and power consumption, while retaining fine frequency resolution [1].

The current trend in synthesizer design is low-power monolithic PLLs for mobile telecommunications applications [2, 3]. These ICs typically use CMOS or BiCMOS processing and employ large feedback-divide ratios, compromising speed and phase noise for low power consumption. As a result, these ICs are poorly suited for low-noise microwave-frequency applications. Although low-noise microwave PLLs have been reported [4], the power consumption exceeded 3W.

We describe a 1W, 5.5GHz, low noise fractional frequency synthesizer–programmer (FSP5) IC that advances the state of the art in high-performance synthesizer design. We fabricated the chip in a 1µm GaAs/AlGaAs HBT process that offers low-noise NPN transistors with $f_t = 43$GHz, $\beta_{dc} = 400$, $LV_{ceo} = 12$V, ~1000V Early voltages, and ~1mV cross-wafer V_{be} matching (1σ). The process includes Schottky-barrier diodes, backside ground vias, selective air-bridge crossovers, 20Ω/□ NiCr resistors, and 300Ω/□ cermet resistors.

II. High-performance frequency synthesizers

Microwave PLL applications typically require high spectral purity (low phase noise and low spurious), fine loop-frequency resolution, and low power consumption. Although synthesizer-IC and PLL designs vary, as a result of design-specification and technology tradeoffs, there are theoretical and practical considerations common to the design of all high-performance synthesizers [1]. Consequently, we begin by reviewing some of the general design and operational characteristics of high-performance synthesizer ICs.

A. Small feedback-path divide ratios

The synthesizer IC's contribution to a PLL's in-band phase noise varies as N/K_ϕ, where N is the feedback-path divide ratio and K_ϕ is the charge-pump gain. Consequently, low-noise PLLs use small N-divide ratios. The FSP5 allows continuously selectable N-divide ratios from 12 to 16383.

B. Fractional synthesis

PLLs with small N values have large tuning steps. To improve the frequency resolution, loop designers use fractional-N synthesis. The FSP5 offers dual-modulus pulse-swallowing fractional synthesis to obtain fine loop-frequency resolution at low N-divide ratios.

C. High charge-pump current

A synthesizer IC's contribution to a PLL's in-band phase noise decreases with increasing charge-pump gain K_ϕ; consequently, low-noise PLLs use high-current charge pumps to tune the voltage-controlled oscillator (VCO). The larger the charge pump's output current, the smaller the path gain for synthesizer IC noise sources (such as divider noise). The FSP5's maximum charge-pump gain is $8\text{mA}/2\pi\text{rad}$.

D. Gain normalization

Tuning a PLL usually involves changing the N-divide ratio. A PLL's loop gain varies with N; consequently, tuning the loop changes the loop gain. To maintain constant loop gain, PLL designers typically adjust another loop parameter when tuning N, thereby ensuring that the PLL's stability margin, loop natural frequency, and noise characteristics remain unchanged with tuned frequency. The FSP5 normalizes the PLL loop gain by adjusting K_ϕ, the charge-pump gain, to compensate the changing N-divide ratios.

E. Noise blanking

A charge pump outputs source-current pulses or sink-current pulses to the loop filter. In the FSP5, the charge-pump output is isolated from the loop filter during the interpulse intervals, blanking the synthesizer IC's noise when the charge pump is not actively sourcing or sinking current.

F. Nonzero phase-detector offset

A PLL with zero phase error neither sources current to, nor sinks current from, the loop filter. Unfortunately, synthesizer ICs with zero phase error are insensitive to small loop-phase deviations, as a result of finite signal rise times in the phase–frequency detector and charge pump. To compensate this zero-phase nonlinearity, loop designers either employ specialized phase–frequency detectors that have no zero-phase dead zone, or they employ simple phase–frequency

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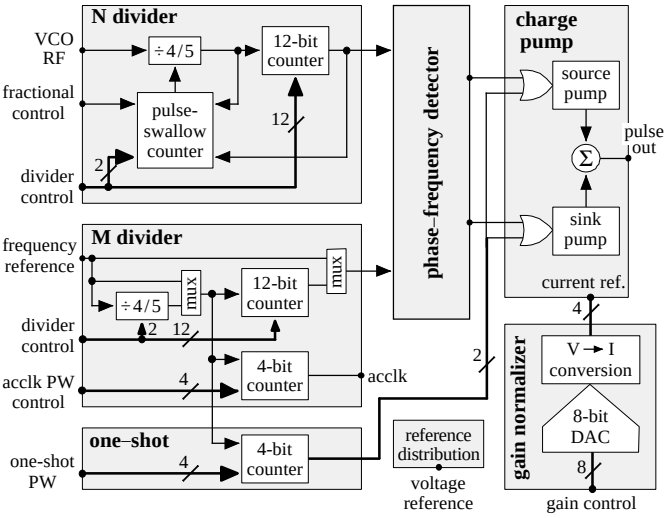
A. The FSP5 Chip Block Diagram



B. A High-Performance Loop Application

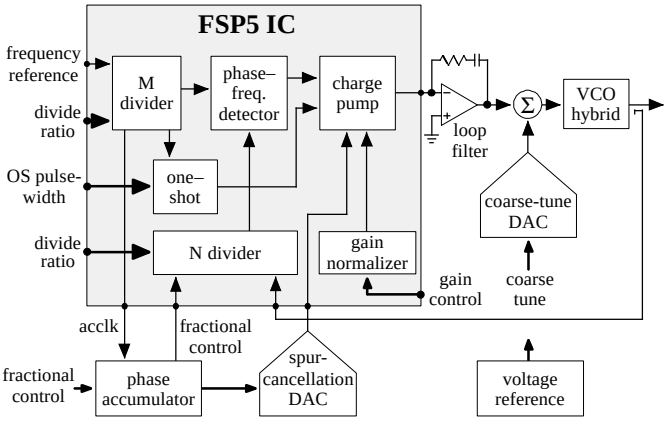


Fig. 1. (A) The FSP5 chip block diagram. We have omitted from this diagram a polarity-inversion multiplexer, that we use to adjust the phase-detector polarity to ensure negative feedback in the PLL; and a line driver / line receiver, that we use in conjunction with an off-chip delay line to (optionally) set the one–shot pulsewidth off chip. (B) A high-performance loop application.

or they employ simple phase–frequency detectors and lock the PLL with an artificial phase offset. The FSP5 uses the artificial phase-offset approach.

III. The FSP5 Frequency-Synthesizer IC

The FSP5 IC is a fractional-N, GaAs/AlGaAs frequency-synthesizer with a 5.5 GHz feedback divider, a 2 GHz reference divider, a programmable one–shot, a 500 MHz phase–frequency detector, a wideband charge pump, and a gain-normalized output current. The chip's power consumption varies from 750 mW to 1.25 W, depending both on bond options that power selected circuitry and on the output current. We show a block diagram of the FSP5 IC in part A of Fig. 1, a loop application in part B, and a die photograph in Fig. 2.

Referring to part A of Fig. 1, the N divider (the feedback divider) allows continuously selectable divide ratios from 12 to 16383, and permits dual-modulus pulse-swallowing (÷N or ÷(N+1)) fractional synthesis with single-bit control. The M

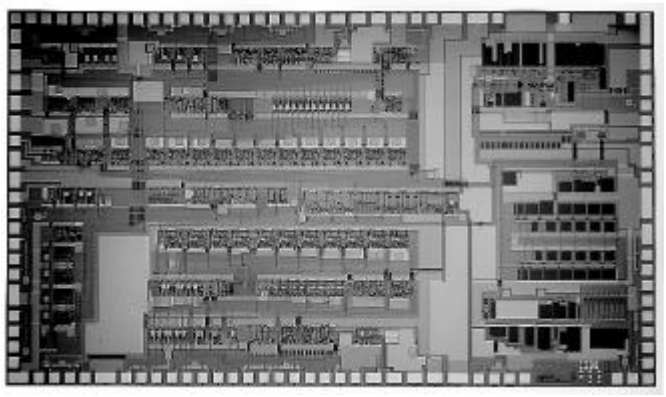


Fig. 2. The FSP5 IC. The chip dimensions are 6350 × 3650 µm. The leftmost two-thirds of the chip is the digital subsection, comprising the N divider, M divider, one–shot, and phase detector. The rightmost third of the chip is the analog subsection, comprising the gain normalizer, V→I conversion and current-mirroring circuitry, reference distribution, and charge pump.

divider (the reference divider) allows continuously selectable divide ratios from 1 to 4095; an optional ÷4/5 input prescaler extends the divide ratios to 20475. The one–shot generates programmable-width pulses at the loop sample frequency, causing the loop to lock with a phase offset outside the zero-phase dead zone. The gain normalizer permits 8-bit control of the charge-pump output current. The charge pump generates sink-current and source-current output pulses as instructed by the one–shot and phase detector. The one–shot typically generates sink pulses; the phase detector, in turn, generates source pulses that, when the loop is locked, cancel the sink pulses at the charge-pump output (see part A of Fig. 5).

The loop application shown in part B of Fig. 1 comprises an FSP5, a phase accumulator to control the fractional-N divider, a loop filter, a spur-cancellation DAC, a coarse-tune DAC, a voltage reference, and a VCO. The spur-cancellation DAC cancels the charge that is injected into the loop filter by the fractional tuning, reducing the output spurs. The coarse-tune DAC pretunes the VCO—although the FSP5 does perform phase–frequency detection, the coarse-tune DAC speeds loop-frequency acquisition. The off-chip VCO and voltage reference ensure low phase noise. In this application, the FSP5 IC consumes 1 W from +5 V and –5.2 V supplies.

The FSP5 IC comprises 1882 transistors, 262 diodes, 1533 resistors, and roughly 250 pF of capacitance distributed across 196 MIM capacitors. The measured yield is 33%. The analog circuitry comprises six op-amps, all compensated internally for 90º of phase margin, that use large-area cermet resistors with 0.1% cross-wafer matching (1σ) to minimize offsets.

We employ current-mode logic (CML) for most of the digital circuitry, with 250 mV differential swings. Unfortunately, the typical V_{be} for a GaAs/AlGaAs NPN transistor is 1.25 V; consequently, we can fit only a four-transistor stack between ground and the –5.2 V supply. Because the current sink and clock each occupy a logic level, we can fabricate only two-input logic gates using standard CML. To enable gates with more than two inputs, we employ a form of diode-transistor logic (DTL) that uses Schottky-barrier diodes and resistors to form logic-summing junctions.

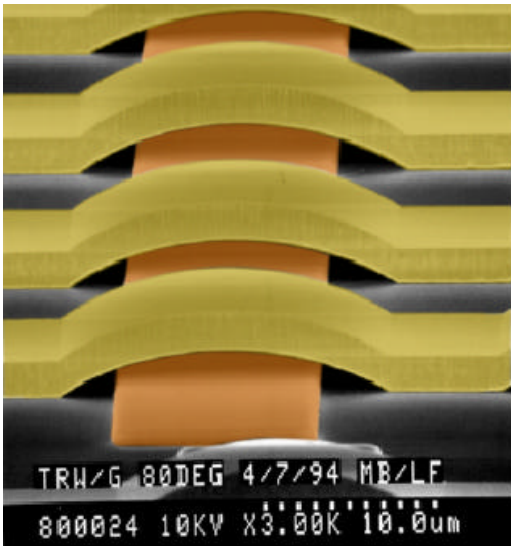


Fig. 3. Top-metal airbridge. To reduce the top-metal trace inductance, we route a small-signal ground strap under the airbridge, as we show in this SEM photo. This ground strap reduces the inductance by 60% to 80%, and doubles the signal propagation velocity, with minimal added capacitance. The typical airbridge trace that we use has a 4μm width, as in this photo.

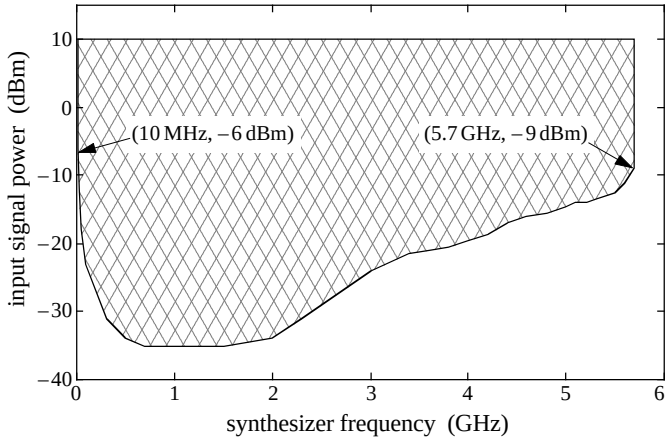


Fig. 4. N-divider (feedback-divider) input sensitivity. We applied a sinusoidal input to the N divider, measured the minimum required input-signal power versus the input frequency, and plotted the input dynamic range (minimum to maximum input power) versus the input frequency. To prevent damaging the IC, the maximum input power is +10 dBm for all frequencies.

In our GaAs/AlGaAs process, the transistor f_t and τ_f achieve their maximum values when V_{cb} is near 0 V: When $V_{cb}>0$ V, the collector-to-base depletion region widens, reducing the speed; when $V_{cb}<0$ V, the stored collector-to-base (diffusion) charge increases, also reducing the speed. Consequently, our digital circuitry maintains $V_{cb}\approx 0$ V wherever possible.

We use controlled-impedance ($z=50\,\Omega$) traces, with resistor terminations, for the N-divider and M-divider RF inputs. We use narrow-width airbridge traces for all high-speed on-chip interconnect—the air dielectric minimizes the capacitive coupling from trace to substrate (by a factor of 1.3 to 2.0, depending on the trace width), and reduces the overlap capacitance in signal crossovers. Minimizing the capacitive load on the signal lines reduces the drive currents, and, consequently, the chip power consumption. We route small-signal ground straps under the airbridge (see Fig. 3), to reduce the series inductance and to increase the signal-propagation velocity. Low inductance minimizes emitter–follower ringing, and high propagation velocity reduces clock skew.

The FSP5's primary subcircuits are an N-divider, M-divider, one–shot and phase–frequency detector, and gain-normalizing charge pump. We now describe each of these subcircuits.

A. The feedback divider (N-divider)

The N-divider is a 14-bit counter comprising an RF preamplifier, a synchronous high-speed divide-by-four/five, and an asynchronous 12-bit ripple counter. The N-divider permits continuously selectable divide ratios from 12 to 16383, and allows dual-modulus pulse-swallowing (÷N or ÷(N+1)) fractional-N synthesis with single-bit control (in fractional mode, the minimum N value is 16). The N-divider's power consumption is roughly 250 mW.

Fractional synthesis permits small N-divide ratios with finer loop-frequency resolution (finer step sizes) than is possible with integer synthesis. The benefit of small N-divide ratios is low in-band phase noise. The disadvantage of fractional synthesis is loop-phase modulation, causing spurs at the PLL output. To reduce the spurs, we use an off-chip spur-cancellation DAC to cancel the charge that is injected into the loop filter by the pulse swallowing. An off-chip phase accumulator commands both this DAC and the N-divider fractional logic (see part B of Fig. 2).

The N-divider's input preamplifier is a three-stage, open-loop, differential (saturating) amplifier with roughly 60 dB of gain. This preamplifier supports differential and single-ended ECL inputs, in addition to ac-coupled sinusoids. We show the preamplifier's input sensitivity, for ac-coupled sinusoidal inputs, in Fig. 4. To prevent noise-induced spurious toggling, the preamplifier requires a minimum input-signal slew rate of roughly 2×10^7 V/s ($z_{source}=50\,\Omega$). For sinusoidal signals, the corresponding minimum input frequency is roughly 10 MHz; for square-wave inputs, the input-frequency range extends much lower than 10 MHz.

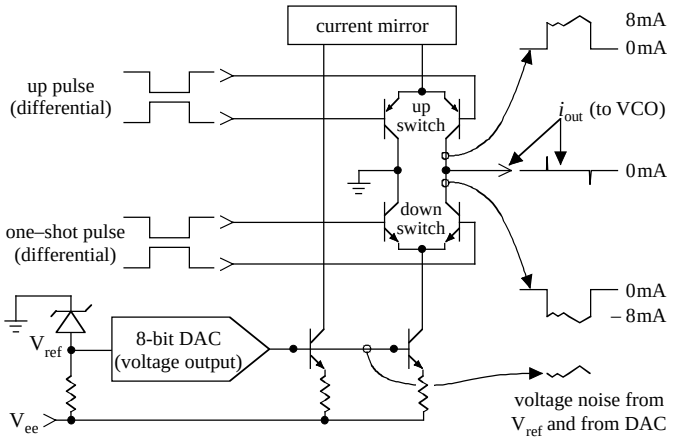
B. The reference divider (M-divider)

The M-divider is a 12-bit counter comprising an RF preamplifier, an asynchronous 12-bit ripple counter, and an optional high-speed divide-by-four/five input prescaler. The M-divider allows continuously selectable divide ratios from 1 to 4095; the optional prescaler extends the divide ratios to 20475. The M-divider's power consumption is roughly 250 mW.

The M-divider sources a TTL-level clock (the accumulator clock, or acclk), at the loop-sample frequency, to the off-chip fractional-phase accumulator. The acclk pulsewidth is four-bit programmable, to ensure compatibility with slower (off chip) TTL circuitry.

The M-divider's input preamplifier is a two-stage, open-loop, differential (saturating) amplifier with roughly 40 dB of gain. This preamplifier supports differential and single-ended ECL inputs, in addition to ac-coupled sinusoids.

A. Pulse Cancellation at the Charge-Pump Output



B. Noise-Cancellation at the Charge-Pump Output

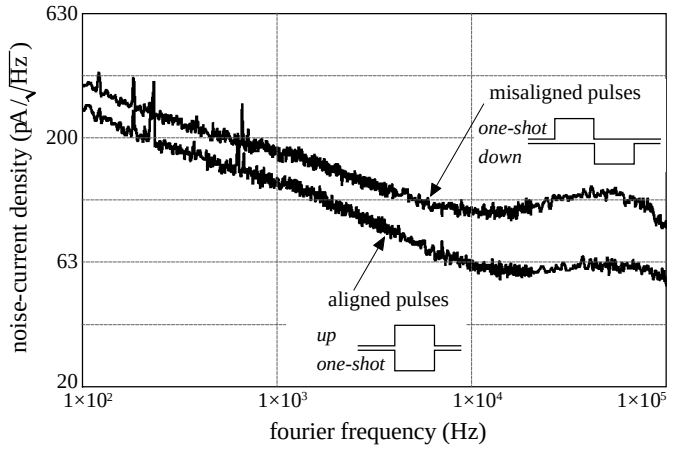


Fig. 5. (A) Pulse cancellation at the charge-pump output. When the PLL is locked, the charge pump's source- and sink-current pulses are aligned and cancel (Note: Our GaAs/AlGaAs process does not have PNP transistors—we show them here for illustration purposes only. The FSP5 emulates a PNP differential pair using active circuits (see Fig. 7)). (B) Measured noise cancellation when the charge-pump pulses were aligned, versus when they were misaligned.

C. The one–shot and phase–frequency detector

The phase–frequency detector generates pulses whose width corresponds to the time differential between the N-divider and M-divider terminal counts. To avoid the phase detector's zero–phase-offset dead zone, we lock our PLLs with an artificial loop-phase offset. We do not generate this offset by injecting a constant (dc) current into the loop filter, because the resulting charge-pump pulses, induced by the loop to compensate the injected (dc) current, cause sample-rate spurs in the VCO output. Instead, we generate this phase offset using a circuit called a one–shot.

A one–shot forces the charge-pump to inject sink-current pulses into the loop filter at the loop sample frequency; the PLL compensates by introducing an artificial loop-phase offset. The phase detector senses this phase offset, and generates source-current pulses to counteract the injected sink-current pulses (see Fig. 5). When the PLL is locked, these source- and sink-current pulses are coincident and cancel at the FSP5 output. Pulse cancellation reduces the signal energy delivered to the loop filter, thereby minimizing sample-rate spurs. In addition, because we derive both the sink and source currents from the same voltage reference and DAC, when the PLL is locked the noise from these sources is coherent and cancels at the charge-pump output.

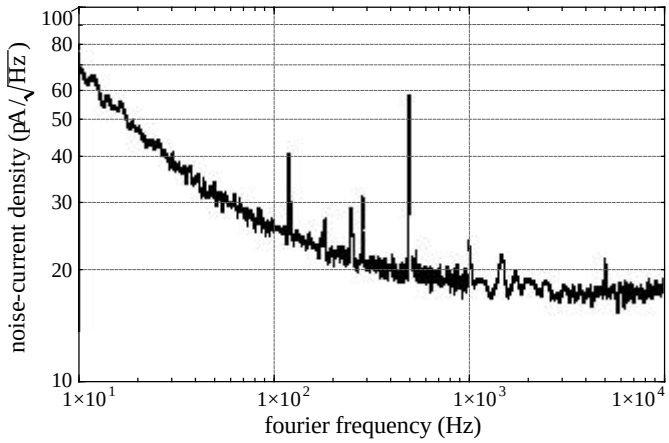


Fig. 6. FSP5 output noise, for typical PLL operating parameters. We repeated the experiment of Fig. 5, with aligned pulses, but we decreased the blanking interval to 98.75% to reduce the noise. We set N to ÷320, $K_\phi = 8\,mA/2\pi\,rad$, $f_{vco} = 1.6\,GHz$, the loop sample period to 200 ns, and the charge-pump output pulsewidth to 2.5 ns. These data remain essentially unchanged for RF power levels (the RF input to the N-divider preamplifier) from –20 dBm to +10 dBm.

To obtain the data in part B of Fig. 5, we constructed a PLL that included an FSP5, the loop filter, and a VCO, and we adjusted the loop parameters so that the dominant noise source below the loop natural frequency was the FSP5 IC. We measured the PLL's output (RF) phase noise in a closed-loop test by beating, in quadrature, the output against the reference frequency, thereby removing the reference noise from the measurement. We re-referenced the noise to the FSP5 output by dividing the data by the in-band loop gain N/K_ϕ, where we set N (the feedback-divide ratio) to ÷320, and K_ϕ (the charge-pump gain) to $8\,mA/2\pi\,rad$. To demonstrate the noise-reducing effects of the pulse cancellation, we set the one–shot pulsewidth to 40 ns (an artificially large value), thereby ensuring that the analog noise (DAC, V_{ref}, and charge-pump noise) was much larger than the digital noise (phase-detector edge jitter) at the charge-pump output. We set the loop sample period to 200 ns; consequently, the noise blanking was 80%.

In typical loop applications, we use one–shot pulsewidths that are much shorter than 40 ns, so the output noise current is much lower than the data in Fig. 5. The FSP5's one–shot pulsewidth is four-bit programmable; a bond option enables an alternative one–shot circuit that uses an off-chip delay line for continuously variable one–shot pulsewidths. In Fig. 6, we show the noise current for a 2.5 ns one–shot pulsewidth. We conducted this test closed-loop; consequently, these data include noise contributions from the entire FSP5, including the phase detector and the charge pump. The one–shot and phase–frequency detector together consume roughly 175 mW.

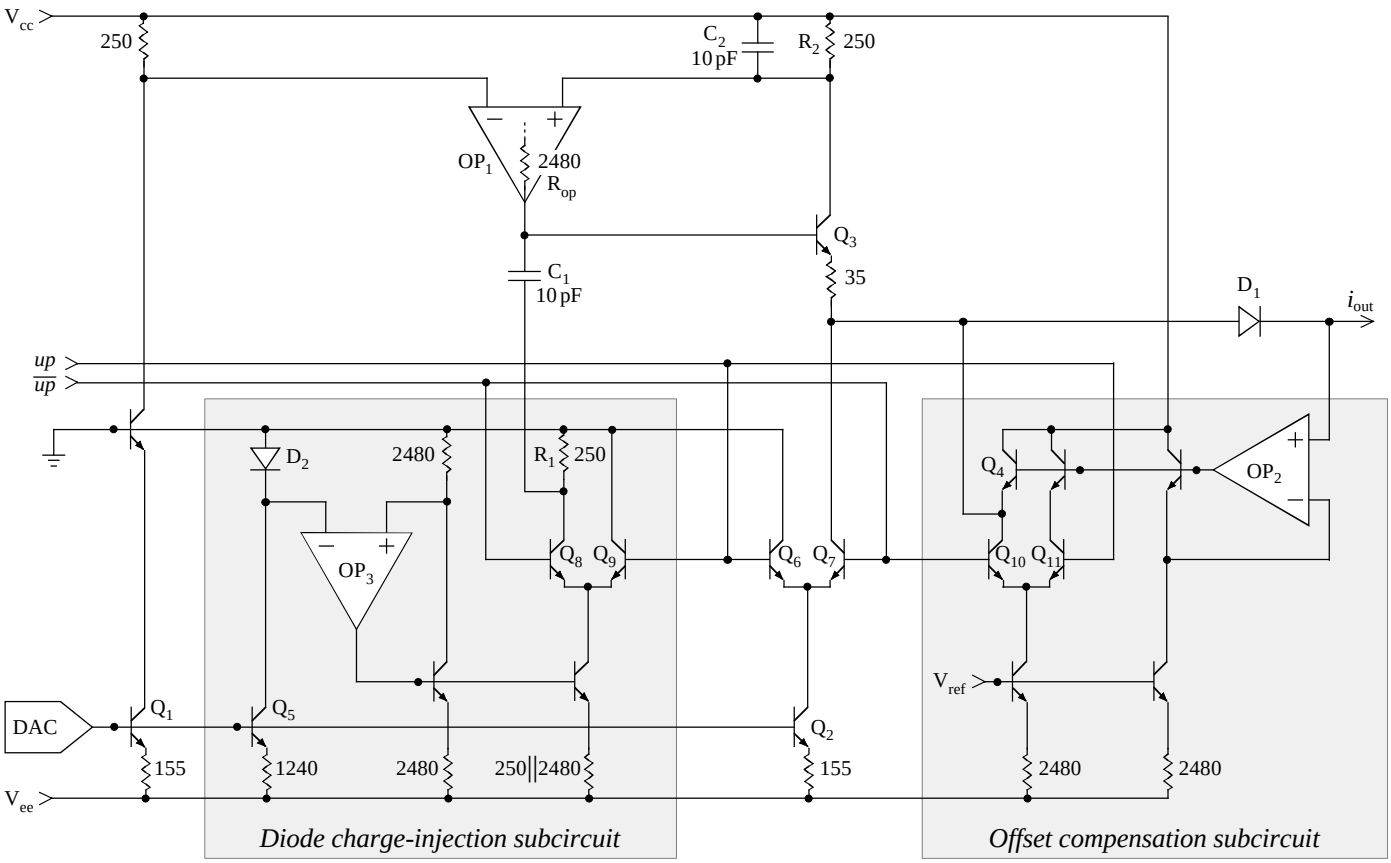


Fig. 7. Source-pump functional circuit diagram. The circuit emulates a PNP differential pair (see Fig. 5), but, owing to the absence of PNP transistors in our production GaAs/AlGaAs process, is considerably more complex. The complete circuit (excluding the DAC) comprises 64 transistors, 14 diodes, 8 capacitors, and 33 resistors. By contrast, the sink pump (not shown here; see Fig. 5) comprises a simple NPN differential pair. The load is a virtual ground, nominally at a 0 V (dc) potential. The source-pump has roughly 60 dB of power-supply rejection, from the +5 V supply to the source-current output.

D. The gain-normalizing charge pump

A PLL's loop gain varies with the N-divide ratio; as a result, tuning the VCO changes the loop gain. In the FSP5, we maintain a constant loop gain by adjusting the charge-pump output current to compensate the changing N-divide ratio, thereby ensuring that the loop stability margin, natural frequency, and noise characteristics remain unchanged with tuned frequency. We derive the charge-pump output current from the N-divide ratio; the control word that sets the N-divide ratio also sets the current in the on-chip 8-bit gain-normalizing DAC.

The FSP5 charge pump comprises a sink-current switch and a source-current switch, as we show in part A of Fig. 5. We fabricate the sink-current switch from an NPN differential pair, as in Fig. 5. Unfortunately, our production GaAs/AlGaAs process does not have PNP transistors; to perform the source-current switching function, we emulate the PNP differential pair using on-chip operational amplifiers.

We show a functional diagram of the source-current switch in Fig. 7. The circuit is an all-NPN, closed-loop, switchable current source comprising three op-amps and several switching differential pairs. The circuit is stable into any value of load capacitance, will drive 8 mA into a virtual ground with a 5 kΩ source impedance, and has <250 ps rise and fall times (simulated) for source-current values from 0.25 mA to 8 mA.

We now describe the detailed operation of this circuit. Current-sink transistors Q_1 and Q_2 sink identical currents, set by the on-chip gain-normalizing DAC. Op-amp OP_1 converts Q_1's sink current into an equivalent source current at Q_3's emitter. We begin by considering the situation when *up* is false. In this condition, the output is isolated from the load by diode D_1. Q_2's sink current, routed to Q_7's collector, cancels the source current at Q_3's emitter; any small error (mismatch) current is removed by transistor Q_4. The offset-compensation subcircuit senses the load voltage, and sets D_1's anode voltage equal to its cathode voltage using transistor Q_4. The diode charge-injection subcircuit calculates D_1's anticipated turn-on voltage, using current source Q_5 and diode D_2, and applies this voltage to resistor R_1.

When *up* switches true, Q_6 turns on, Q_7 turns off, and Q_3's emitter current now drives D_1's anode. Simultaneously, Q_9 turns on, Q_8 turns off, and resistor R_1 pulls Q_3's base high, through capacitor C_1, by an amount calculated previously (by Q_5 and D_2) to turn D_1 on rapidly with an anode voltage that is commensurate with Q_3's emitter current. Op-amp OP_1 corrects errors in i_{out}, with a 1 GHz closed-loop bandwidth (nominal conditions, with i_{out}=4 mA). Also, Q_{10} turns off, Q_{11} turns on, and Q_4 no longer drives D_1's anode. Because of the rapid charge injection into Q_3's base, D_1 turns on (and off) in 250 ps (simulated), for source-current values ranging from 0.25 mA to 8 mA. Furthermore, with the exception of tran-

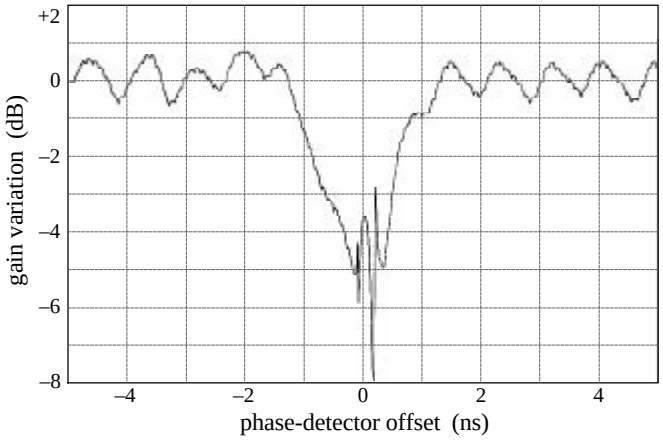


Fig. 8. FSP5 gain variation. We constructed a PLL using an FSP5, injected an FM tone into the loop, swept the loop-phase offset bidirectionally around the zero–phase-offset gain null, and measured the tone amplitude at the loop output. We plotted the tone amplitude (normalized to the mean value outside the gain null) versus the phase offset. The gain ripple is roughly ±0.5 dB; the null width and depth are roughly ±1 ns and 4.5 dB, respectively.

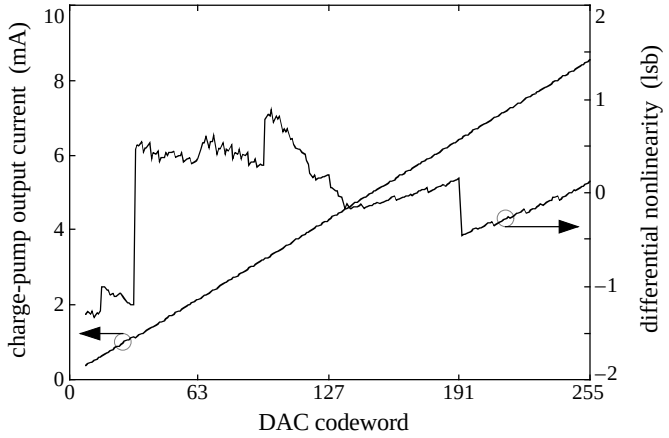


Fig. 9. Gain-normalizer linearity. We measured the charge-pump sink current versus the gain-normalizer DAC codeword, and plotted both the output current and the differential nonlinearity versus the codeword. The full-scale output current was 8.53 mA, the RMS level errors were 0.49 lsb (least-significant bits), and the maximum level error was 1.33 lsb. The analog circuitry does not support codewords smaller than 8 (output currents smaller than about 0.25 mA).

sient glitch energy, transistor Q_3 sources a constant current, regardless of whether *up* is false or true.

Capacitor C_1 and resistor R_{op} form a dominant pole in OP_1's compensation; the lead–lag network comprising C_1, R_{op}, and R_1 discards roughly 20 dB of loop gain. A second pole, formed by C_2 and R_2, ensures that OP_1's loop gain crosses unity with at least 80° of phase margin (worst case, simulated). Finally, OP_2's input bias current is about 250 nA.

Op-amp OP_1 and transistor Q_3 set the source pump's output current. Because Q_3's small-signal emitter impedance increases with decreasing output current, the open-loop gain of the OP_1–Q_3 loop decreases with decreasing output current. Consequently, the loop bandwidth decreases and the loop error increases for small output currents; to ensure accuracy and settling, we restrict the minimum gain-normalizer DAC current to 0.25 mA. The FSP5's output-current range extends from ±0.25 mA to ±8 mA, in 31.25 µA steps. The FSP5 permits gain normalization over a 32:1 VCO tuning range; most applications tune over a 8:1 or smaller range.

The charge pump's composite output (source-current switch and sink-current switch) has a ±1 V compliance with a ±8 mA output current. The gain normalizer and charge pump together consume roughly 325 mW.

IV. FSP5 Performance

We have probe tested roughly 100 working FSP5 die, and we have performed detailed testing on 10 packaged parts; the data we show here represents typical FSP5 performance. We show N-divider sensitivity data in Fig. 4. The N-divider operates to 5.7 GHz, requiring only a –15 dBm input at 5 GHz. As a result of the divider's speed and sensitivity, we can divide microwave frequencies directly, without RF downconversion, using direct feedback from the VCO to the N-divider.

The TTL input buffers that accept the N-divide command word (that sets the N-divide ratio) have 50 MHz bandwidths, thereby allowing us to directly modulate the FSP5's N-divide ratio at loop sampling rates up to 50 MHz. We have fabricated fractional PLLs, using an FSP5 IC, that sigma-delta modulate [5] the N-divide ratio at 10 MHz.

In the experiment of Fig. 5, we set the charge-pump duty cycle to 20% (i.e., we set the noise blanking to 80%). We did this so that analog noise, rather than divider edge jitter, was the dominant noise source at the chip output, thereby enabling us to measure accurately the noise reduction due to pulse alignment. In Fig. 6, we show FSP5 noise in a typical application, with 98.75% noise blanking. Because the noise floor is only $18\,\text{pA}/\sqrt{\text{Hz}}$, and because the gain normalization ensures fixed loop gains, we can design wideband PLLs that suppress the phase noise from other sources (such as the VCO) and have fast settling.

We show closed-loop PLL gain-variation data in Fig. 8. On the basis of the gain-null width, the minimum usable phase-detector offset is roughly ±1 ns. As a result, the maximum usable phase-detector frequency is 500 MHz. The ±0.5 dB passband ripple (at the M-divider's input (RF) frequency) provides a measure of isolation in the phase-frequency detector: The ripple is caused by the reference signal (M-divider RF) coupling onto the feedback divider (N-divider) signal path in the phase–frequency detector.

We show gain-normalizer linearity data in Fig. 9. We measured these data at the charge-pump output, using a 100% pulse duty cycle (no noise blanking); they demonstrate 8-bit accuracy in the gain normalizing DAC. The DAC is a 3-bit segmented, 5-bit R–2R design; the principal linearity errors occur at the carry transitions, where the R–2R counter rolls over (e.g. at a codeword of 31).

The M-divider's input-frequency range, for sinusoidal inputs, is 10 MHz to 500 MHz without the ÷4/5 input prescaler, and is 10 MHz to 2 GHz with the prescaler. The preamplifier's input sensitivity allows –10 dBm RF inputs (+10 dBm maximum) from 10MHz to 1.2GHz. For square-wave inputs, the frequency range extends much lower than 10 MHz.

Finally, the FSP5 IC operates over a –55°C to +125°C temperature range, with ±5% supply variations.

V. Conclusion

We have demonstrated a 5.5 GHz GaAs/AlGaAs frequency-synthesizer IC with dual-modulus pulse-swallowing fractional synthesis, 18 pA/$\sqrt{\text{Hz}}$ noise-current spectral density, and 1 W power consumption. The FSP5 advances the state-of-the-art in high-performance microwave frequency synthesizers. The chip's most significant features are ultra-low noise at moderate power consumption, and the ability to divide microwave frequencies directly (without RF downconversion). The low noise allows us to construct PLLs with wideband loops, thereby suppressing the noise from other sources (such as the VCO) and reducing the loop settling times. We anticipate using the FSP5 in high-performance, phase-noise and settling-time sensitive microwave telecommunications applications.

We have isolated the FSP5's noise sources experimentally, and we have found that the dominant noise source is edge jitter in the one–shot circuitry. We are iterating the design, and we expect a 10 pA/$\sqrt{\text{Hz}}$ noise floor with a redesigned chip.

VI. References

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