

# Contemporary Logic Design, 2<sup>nd</sup> Edition

## Errata as of 28 September 2005

### Front Matter

None reported so far.

### Chapter 1

Page 2: the “20mm” measurement in Figure 1.1 is incorrect and should be corrected.

Page 26: 5<sup>th</sup> line from the top has the misspelled word “hinted”.

### Chapter 2

Page 57: last sentence of 1<sup>st</sup> paragraph should read “There is only one way to do it.”

Page 73: in the derivation of  $F'$ , the 2<sup>nd</sup> second line labeled with “DeMorgan's law” is erroneous and should just be deleted.

Page 87: problem 2.19(a) should say “... in canonical minterm form, that is, using product terms of 4 literals each.”; problem 2.19(b) should say “... in canonical maxterm form, that is, using sum terms of 4 literals each.”; problem 2.19(c) should say “... and in canonical minterm form.”; problem 2.19(d) should say “... and in canonical maxterm form.”

Page 88: problem 2.23(a), the last sentence should read “For this part, make sure to use “little  $m$ ” notation.

### Chapter 3

Page 100: the two bottom right cells (not circled) of the K-map in Figure 3.8 should both have values of 0 and not 1.

Page 107: the vertical blue lines in Figure 3.14 are not drawn correctly. The figure should look like this:

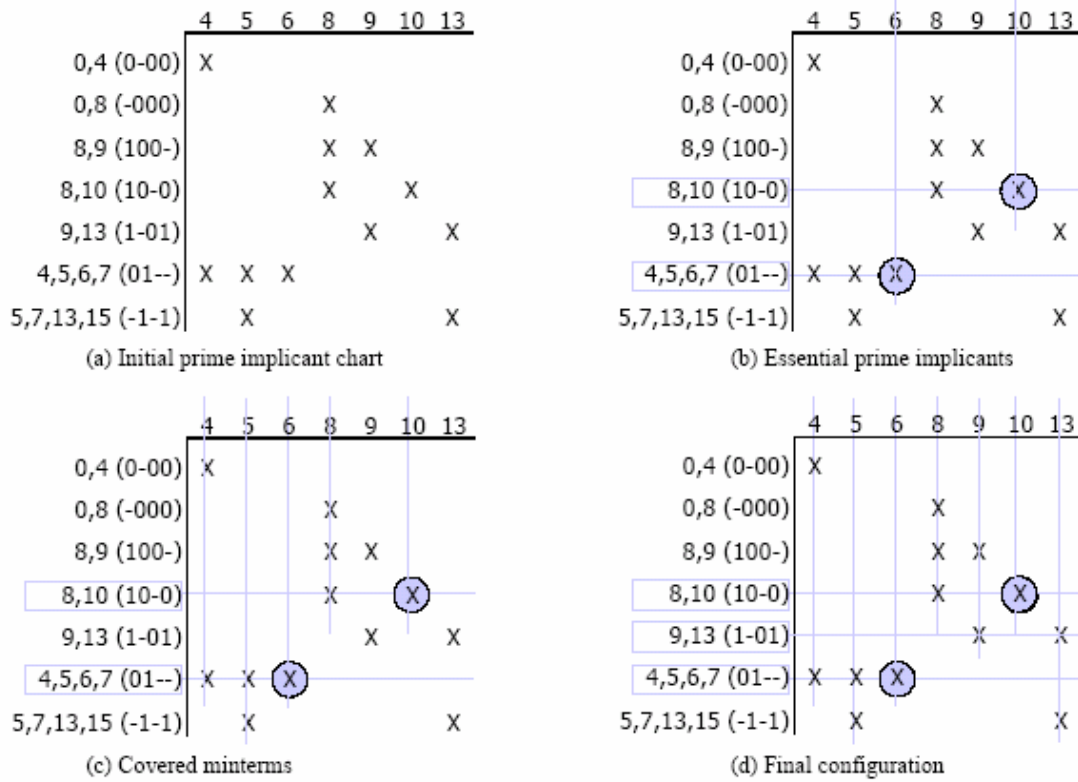


Figure 3.14 The prime implicant chart.

- Page 124:  $B_{in}$  in the equations for G1 and G2 at the top of the page should be just B.
- Page 125: the slash after the D in the equation for Z should be removed.
- Page 129: in the third paragraph's 2<sup>nd</sup> sentence "an script" should be "a script".
- Page 134: in the schematic on the right hand side of Figure 3.42, the D input to gate G2 should have a value of 1, not 0.
- Page 142: the two italicized "always" in the middle paragraph should be in "code" font.
- Page 142: "if (a) then z = ..." in the middle of the page should be "if (a) z = ...".
- Page 144, the two module descriptions at the bottom of the page visually appear to overlap each other, there should be a more clear separation between them.
- Page 146: in the first line at the top of the page, "continuous" is misspelled.
- Page 149: in problem 3.13 replace "Section 3.4.1" with "Example 3.12 in Section 3.4.1" and replace "Section 2.2" with "Example 2.3 in Section 2.2.2".
- Page 150: remove the last right parenthesis from the equation for F in problem 3.17. Start the equation for H on a new line and remove the semicolon (;) after the equation for G.

Page 151: Both parts of Figure Ex3.19 have minor errors. The top NAND in part (a) of the figure has a sort of shadow line at the top that should not be there. In part (b) the last major interval has 6 sub intervals rather than 5 like all the others. They should all match.

## Chapter 4

Page 196: 2<sup>nd</sup> to last sentence before the start of Section 4.2, should say "... onto a single chip and by observing which functions designers find themselves implementing most often."

Page 210: in Figure 4.55 there be a dot at the intersection of the address busses of U3 and U1 with A12:A0. A12:A0 is connected to the inputs of all 4 ROMs.

## Chapter 5

Page 228: there are errors in the Verilog description of the KeypadDecoder. Note the "or" instead of ",", in the sensitivity list of the always block; the correct binary number notation of, for example, 3'b001; the parentheses around the conditional parts of the if statements; and the additional register declaration for KP. It should be:

```
module keypaddecoder (R1, R2, R3, R4, C1, C2, C3, K8, K4, K2, K1, KP);
    input      R1, R2, R3, R4, C1, C2, C3;
    output     K8, K4, K2, K1, KP;
    reg[3:0]   key;
    reg        KP;

    always @(R1 or R2 or R3 or R4 or C1 or C2 or C3) begin
        key = 3'bxxx; // default value for key, will be set if KP is true
        if (R1 & C1) key = 1;
        if (R1 & C2) key = 2;
        if (R1 & C3) key = 3;
        if (R2 & C1) key = 4;
        if (R2 & C2) key = 5;
        if (R2 & C3) key = 6;
        if (R3 & C1) key = 7;
        if (R3 & C2) key = 8;
        if (R3 & C3) key = 9;
        if (R4 & C1) key = 10;
        if (R4 & C2) key = 0;
        if (R4 & C3) key = 15;
        KP = ((R1 + R2 + R3 + R4) == 3'b001)
            && ((C1 + C2 + C3) == 3'b001);
    end

    assign K8 = key[3];
    assign K4 = key[2];
    assign K2 = key[1];
    assign K1 = key[0];
endmodule
```

Page 230: three lines above the equations at the bottom of the page, the phrase "see if it possible" should be "see if it is possible".

Page 235: in the Verilog in the middle of the page, “3b” should be replaced by “3'b” in all 8 instances.

Page 243: in the 2<sup>nd</sup> to last line, “computer” should be “compute”.

Page 244: in the 2nd sentence of the 2nd full paragraph “Using the schematics of Figure 5.16 ...” should be “Using the schematics of Figure 5.18 ...”.

Page 248: in Figure 5.23’s caption, “drived” should be “derived”.

Page 255: in problem 5.4(a) add the following sentences after the first and before “Use ...”: “For example, suppose we have March 15, then MONTH = 3 and the OFFSET into the year is  $31 + 28 = 59$ . This is what will be added to DAY = 15 for a day-of-the-year of  $59 + 15 = 74$ . If it was a leap year, then it would be 75.”

## **Chapter 6**

Page 275: in the last sentence of 2<sup>nd</sup> paragraph under “Latches and flip-flops” there is the word “elment” that should be “element”.

Page 298: last sentence before the Chapter Review should be “The values of *out* are...”.

## **Chapter 7**

Page 339: last sentence of 2<sup>nd</sup> paragraph should end with “how don't cares were used”.

Page 343: a close quotation (”) needs to added to the end of “... decisions.” (the 1<sup>st</sup> paragraph).

Page 343: the last sentence of the paragraph between the input/output and state descriptions has an extra “had” and should be “Thus, there are four major states for the controller has that may need to be further refined into individual states.”

Page 344: 3<sup>rd</sup> line should be “We can do this by having ...”.

## **Chapter 8**

Page 355: in the 2<sup>nd</sup> line of the 3<sup>rd</sup> paragraph “braking” should “breaking”.

Page 371: the 1<sup>st</sup> line of the 4<sup>th</sup> paragraph of section 8.2.3 should read “... is shown in Figure 8.25.”

Page 396: the caption for Figure Ex 8.11 should read “Next-state functions for Exercises 8.11 and 8.12.”

Page 396: the table in Figure Ex 8.11 is wrong and needs to be replaced with the one below. The text of Exercises 8.11 and 8.12 should read:

8.11 (State Reduction) Given the next-state function of the finite state machine shown in Figure Ex. 8.11, find the most reduced state diagram. The state machine has four state bits, 1 input, and 1 output (the output is asserted only in states 0, 2, 4, 6, 7, 8, 10, 12, 14, and 15).

8.12 (State Partitioning) Partition the next-state functions of the reduced state machine of Exercise 8.11 into two parts that compute two outputs each but having no more than 4 inputs to each part.

Q3	Q2	Q1	Q0	In	P3	P2	P1	P0
0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	1	1	0
0	0	0	1	0	0	0	1	0
0	0	0	1	1	0	0	0	1
0	0	1	0	0	0	0	1	1
0	0	1	0	1	0	1	0	0
0	0	1	1	0	0	1	0	0
0	0	1	1	1	0	0	1	1
0	1	0	0	0	0	1	0	1
0	1	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	0
0	1	0	1	1	1	0	0	0
0	1	1	0	0	0	0	1	1
0	1	1	0	1	0	1	1	1
0	1	1	1	0	0	1	0	1
0	1	1	1	1	0	0	0	0
1	0	0	0	0	1	0	0	1
1	0	0	0	1	1	1	1	0
1	0	0	1	0	1	0	1	0
1	0	0	1	1	1	0	0	1
1	0	1	0	0	1	0	1	1
1	0	1	0	1	1	1	0	0
1	0	1	1	0	1	1	0	0
1	0	1	1	1	1	0	1	1
1	1	0	0	0	1	1	0	1
1	1	0	0	1	1	0	0	0
1	1	0	1	0	1	0	0	0
1	1	0	1	1	1	0	1	1
1	1	1	0	0	1	1	1	1
1	1	1	0	1	1	1	1	1
1	1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	0	0

**Chapter 9**

Page 450: in problem 9.18, 25-input parity function should be a 16-input parity function.

**Chapter 10**

Page 505: in problem 10.7, Section 8.5.4 should be Section 10.3.

Page 505: in problem 10.10, Section 7.6.5 should be Section 10.4.5.

Page 505: in problem 10.11, Figures 7.55 and 7.56 should be Figures 10.24 and 10.25.

### **Appendix A**

Page 511: 2<sup>nd</sup> paragraph, 2<sup>nd</sup> sentence, should be "... We have 10 digits on our hands (8 fingers and 2 thumbs) – we had digits before we had numbers! However, a base-10 system is not natural ..."

Page 527: in the text above the additions, there is a missing "Ca" that for "rry-in" over the first example. The right-most edge of the binary additions is cut off abruptly.

### **Appendix B**

Page 565: in problem B.4, "AVLC" should be "ALVC".

Page 565: in problem B.6, the power units for CMOS technology should be "micro-watts" or " $\mu\text{W}$ " rather than "milli-watts" or "mW" – that is, 0.5mW is ok, but "30mW + 750mW" should be " $30\mu\text{W} + 750\mu\text{W}$ ".

### **Appendix C**

None reported so far.