Lawrence Snyder

Curriculum Vita

Education:

PhD -- 1973 Carnegie Mellon University -- Computer Science (A.N. Habermann, advisor)
BA -- 1968 University of Iowa -- Mathematics and Economics

Professional Experience:

Professor of Computer Science and Engineering, University of Washington, 1983 --
Visiting Professor, University of Sydney, 1994 - 1995
Visiting Scholar, MIT and Harvard, 1987 - 1988
Professor of Computer Sciences, Purdue University, 1983
Associate Professor of Computer Sciences, Purdue University, 1980 - 1983
Visiting Scholar, University of Washington, 1979 - 1980
Associate Professor of Computer Science, Yale University, 1978 - 1980
Assistant Professor of Computer Science, Yale University, 1973 - 1978

Recognition:

Fellow of the IEEE for "Contributions to parallel computer programming, computer architecture and the theoretical foundations of computer science," 1992
Fellow of the ACM, 1994

Recent Professional Service:

General Co-Chair, International Symposium on Computer Architecture, 1990
Chair, Advisory Council, CS Department, Princeton University, 1995 - (Member, 1989 -)
Chair, Advisory Committee, CS Department, Oregon Graduate Institute, 1995 - (Member, 1988 -)
Member, Program Committee, Second Conference Principles and Practices of Parallel Programming, 1990
Member, Advisory Committee for Science and Technology Centers, NSF, 1990 - 1992
Chair, External Review Committee, CS Department, Pennsylvania State University, 1990
Member, School of Computer Science Advisory Panel, Carnegie Mellon University, 1991-1998
General Chair, Symposium on Parallel Algorithms and Architectures, 1991 - 1994
External Reviewer, CS Department, University of Utah, 1992
Chair, National Research Council CSTB Committee on Academic Careers in Experimental Computer Science, 1992 - 1994
Member, External Review Committee, CIS and CE Departments, University of California, Santa Cruz, 1992
Member, External Review Committee, Math and CS Department, Dartmouth University, 1993
Member, Final Selection Panel, CISE High Performance Computer and Communication Initiative, NSF, 1993
General Chair, Symposium on Integrated Systems, 1993
Organizer, Parallel Computer Routing and Communication Workshop, 1994
Member, External Review Committee, CS Department, University of Texas, Austin, 1995
Member, CISE Review Panel for CCR and MIPS Divisions, NSF, 1995
Board Member, National Research Council's Army Research Laboratory Technical Assessment Board, 1996 --
Organizer, NSF Workshop on Experimental Research in Computer Science, 1996
Board Member, Computer Research Association, 1996 --
Chair, CSTB Committee on Computer Literacy, National Research Council, 1997 - 1999
Member, CISE Panel on Future Directions in Experimental Computer Science, 1998

Recent Books:

Academic Careers in Experimental Computer Science and Engineering, National Academy Press, 1994
A Programmer's Guide to ZPL, MIT Press, 1999
Being Fluent With Information Technology, National Academy Press, 1999
Fluency With Information Technology, 2000 (draft)

Recent Doctoral Students:

Samuel William Ho, *Formal Models in Computer Architecture*, 1991
Smaragda Konstantinidou, *Deterministic and Chaotic Adaptive Routing in Multicomputers*, 1991
David Grimes Socha, *Supporting Fine-grain Computation on Distributed Memory Parallel Computers*, 1991
Calvin Lin, *The Portability of Parallel Programs Across MIMD Computers*, 1992
Kevin Winn Bolding, *Chaotic Routing -- Design and Implementation of an Adaptive Multicomputer Network Router*, 1993
Ton Ahn Ngo, *The Role of Performance Models in Parallel Programming and Languages*, 1997
Melanie Lewis Fulgham, *Multicomputer Routing Techniques*, 1997
Sung-Eun Choi, *Machine Independent Communication Optimizations*, 1999
Wilbert Derrick Weathersby, *Machine Independent Compiler Optimizations for Collective Communication*, 1999

Selected Refereed Publications:

On Uniquely Represented Data Structures, *18th IEEE Found. Of Comp. Sci.*, pp. 142-156, 1977
Optimal 2-3 Trees, with R. Miller, N. Pippenger, A. Rosenberg, *SIAM J Comp.* 8(1):42-59, 1979
Formal Models in the Take/Grant Protection Model, *J Comp. Sys. Sci* 23(3):333-347, 1981
Introduction to the Configurable, Highly Parallel (CHiP) Computer, *IEEE Computer* 15(1):47-56, 1982
Perfect Storage Representations for Families of Data Structures, with F. Chung, A. Rosenberg *SIAM J Alg. & Discrete Structures* 4(4):548-565, 1983
Parallel Programming and the Poker Programming Environment, *IEEE Computer* 17(7):27-36, 1984
Testing the Coordination Predicate, with J. Cuny, *IEEE Trans. on Computers* 33(3):201-208, 1984
Systolic Architectures - A Wafer Scale Approach, with K. Hedlund, IEEE *Proc. Int'l Conf. On Comp. Design: VLSI in Computers*, pp. 604-610, 1984
The Quarter Horse I: A Case Study in Rapid Prototyping of a 32-bit Microprocessor Chip, with S. Ho, B. Jinks, T. Knight, J. Schaad, A. Tyagi and C. Yang, *IEEE Proc. Int'l Conf. On Comp. Design: VLSI in Computers*, pp. 261-266, 1985
Type Architecture, Shared Memory and the Corollary of Modest Potential, *Annual Review of Computer Science, Vol. 1*, Annual Reviews, 1986
The Hough Transform Has O(N) Complexity on NxN Mesh Connected Computers, with R. E. Cypher, J. L. C. Sanz, *SIAM J. Computing* 19(5):805-820, 1990
Generalized Planar Matchings, with F. Berman, D. Johnson, T. Leighton, P. Shor, *J Algorithms*, 11:153-184, 1990
Chaos Router: Architecture and Performance, with S. Konstantinidou, *18th ISCA*, pp. 212-221, 1991
Chaos Router Patent, US Patent No. 5,151,900, 1992
The Case for Chaotic Adaptive Routing, with K. Bolding, M. Fulgham, *IEEE Transactions on Computers* 46(12):1281-1291, 1997
ZPL's WYSIWYG Performance Model, with B. Chamberlain, S-E. Choi, E Lewis, C. Lin, and W. Weathersby, *Proc. IEEE Workshop on High-level Programming Models*, pp. 50-61, 1998
Abstractions for Portable, Scalable Parallel Programming, with G. Alverson, W. Griswold, C. Lin, D. Notkin, *IEEE Trans. on Parallel and Distributed Systems* 9(1):71-86, 1998
ZPL: A Machine Independent Language for Parallel Computers, with B. Chamberlain, S-E Choi, E Lewis, C. Lin, W. Weathersby, *IEEE Trans. on Software Engineering*, (to appear)