Luis Vega

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Education

University of Washington. Seattle, WA
Ph.D., Computer Science & Engineering, (Expected: 2022)
Advisor: Luis Ceze and Dan Grossman

University of Washington. Seattle, WA
M.S., Computer Science & Engineering, 2021

University of Kaiserslautern. Germany
M.S., Electrical & Computer Engineering, 2014

University of Los Andes. Venezuela
B.S., Electrical Engineering, 2010

Employment

OctoML, Seattle, WA
Research Intern, January 2020 – Present

Microsoft Research, Redmond, WA
Research Intern, June 2018 – August 2018

University of California San Diego, San Diego, CA
Staff Research Associate, April 2013 – September 2017

University of Kaiserslautern, Germany
Research Assistant, January 2012 – March 2013

Publications

Refereed Conference and Journal Papers

Reticle: A Virtual Machine for Programming Modern FPGAs
Luis Vega, Joseph McMahan, Adrian Sampson, Dan Grossman, and Luis Ceze
Programming Language Design and Implementation (PLDI) 2021

LastLayer: Towards Hardware and Software Continuous Integration
Luis Vega, Jared Roesch, Joseph McMahan, and Luis Ceze
IEEE Micro 2020

Evaluating Celerity: A 16nm 695 Giga-RISC-V Instructions/s Manycore Processor with Synthesizable PLL
Austin Rovinski, Chun Zhao, Khalid Al-Hawaj, Paul Gao, Shaolin Xie, Christopher Torng, Scott Davidson, Aporva Amarnath, Luis Vega, Bandhav Veluri, Anuj Rao, Tutu Ajayi, Julian Puscar, Steve Dai, Ritchie Zhao, Dustin Richmond, Zhiru Zhang, Ian Galton, Christopher Batten, Michael B. Taylor, and Ron G. Dreslinski
IEEE Solid-State Circuits Letters 2019

A Hardware-Software Blueprint for Flexible Deep Learning Specialization
Thierry Moreau, Tianqi Chen, Luis Vega, Jared Roesch, Lianmin Zheng, Eddie Yan, Josh Fromm, Ziheng Jiang, Luis Ceze, Carlos Guestrin, Arvind Krishnamurthy
IEEE Micro 2019

A 1.4 GHz 695 Giga RISC-V Inst/s 496-core Manycore Processor with Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS
Austin Rovinski, Chun Zhao, Khalid Al-Hawaj, Paul Gao, Shaolin Xie, Christopher Torng, Scott Davidson, Aporva Amarnath, Luis Vega, Bandhav Veluri, Anuj Rao, Tutu Ajayi, Julian Puscar, Steve Dai, Ritchie Zhao, Dustin Richmond, Zhiru Zhang, Ian Galton, Christopher Batten, Michael B. Taylor, and Ron G. Dreslinski
IEEE Symposium on VLSI Technology and Circuits 2019

Extreme Datacenter Specialization for Planet-Scale Computing: ASIC Clouds
Shaolin Xie, Scott Davidson, Ikuo Magaki, Moein Khazraee, Luis Vega, Lu Zhang, and Michael B. Taylor
ACM SIGOPS Operating Systems Review 2018

Hiding Intermittent Information Leakage with Architectural Support for Blinking
Alric Althoff, Joseph McMahan, Luis Vega, Scott Davidson, Timothy Sherwood, Michael B. Taylor, and Ryan Kastner
International Symposium on Computer Architecture (ISCA) 2018

The Celerity Open-Source 511-Core RISC-V Tiered Accelerator Fabric: Fast Architectures and Design Methodologies for Fast Chips
Scott Davidson, Shaolin Xie, Christopher Torng, Khalid Al-Hawaj, Austin Rovinski, Tutu Ajayi, Luis Vega, Chun Zhao, Ritchie Zhao, Steve Dai, Aporva Amarnath, Bandhav Veluri, Paul Gao, Anuj Rao, Gai Liu, Rajesh K. Gupta, Zhiru Zhang, Ronald G. Dreslinski, Christopher Batten, and Michael B. Taylor
IEEE Micro 2018

Celerity: An Open-Source RISC-V Tiered Accelerator Fabric
Tutu Ajayi, Khalid Al-Hawaj, Aporva Amarnath, Steve Dai, Scott Davidson, Paul Gao, Gai Liu, Atieh Lotfi, Julian Puscar, Anuj Rao, Austin Rovinski, Loai Salem, Ningxiao Sun, Christopher Torng, Luis Vega, Bandhav Veluri, Xiaoyang Wang, Shaolin Xie, Chun Zhao, Ritchie Zhao, Christopher Batten, Ronald G. Dreslinski, Ian Galton, Rajesh K. Gupta, Patrick P. Mercier, Mani Srivastava, Michael B. Taylor, and Zhiru Zhang
Hotchips 2017

Specializing a Planet's Computation: ASIC Clouds
Moein Khazraee, Luis Vega Gutierrez, Ikuo Magaki and Michael Bedford Taylor
IEEE Micro 2017

Moonwalk: NRE Optimization in ASIC Clouds
Moein Khazraee, Lu Zhang, Luis Vega and Michael Bedford Taylor
Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2017

ASIC Clouds: Specializing the Datacenter
Ikuo Magaki, Moein Khazraee, Luis Vega Gutierrez and Michael Bedford Taylor
International Symposium on Computer Architecture (ISCA) 2016

Workshops, Invited Papers, Short Papers, and Extended Abstracts

ASIC clouds: specializing the datacenter for planet-scale applications
Michael Bedford Taylor, Luis Vega, Moein Khazraee, Ikuo Magaki, Scott Davidson, Dustin Richmond
Communications of the ACM 2020

Relay: A High-Level Compiler for Deep Learning
Jared Roesch, Steven Lyubomirsky, Marisa Kirisame, Logan Weber, Josh Pollock, Luis Vega, Ziheng Jiang, Tianqi Chen, Thierry Moreau, and Zachary Tatlock
arXiv preprint 1904.08368 (Technical Report) 2019

RV-IOV: Tethering RISC-V Processors via Scalable I/O Virtualization.
Luis Vega and Michael Bedford Taylor
Computer Architecture Research with RISC-V (CARRV) 2017

Experiences Using the RISC-V Ecosystem to Design an Accelerator-Centric SoC in TSMC 16nm
Tutu Ajayi, Khalid Al-Hawaj, Aporva Amarnath, Steve Dai, Scott Davidson, Paul Gao, Gai Liu, Anuj Rao, Austin Rovinski, Ningxiao Sun, Christopher Torng, Luis Vega, Bandhav Veluri, Shaolin Xie, Chun Zhao, Ritchie Zhao, Christopher Batten, Ronald G. Dreslinski, Rajesh K. Gupta, Michael B. Taylor, and Zhiru Zhang
Computer Architecture Research with RISC-V (CARRV) 2017

Power Side Channels in Security ICs: Hardware Countermeasures
Lu Zhang, Luis Vega, and Michael Taylor
arXiv preprint 1605.00681 (Technical Report) 2016

Teaching

Teaching Assistant

- Winter 2019 – UW CSE 351: The Hardware and Software Interface (Undergraduate)
- Spring 2018 – UW CSE 548: Computer System Architecture (Graduate)

Awards

- IEEE Micro Best Paper Award, for VTA, 2019.
- IEEE Micro Top Picks from the Computer Architecture Conferences, for ASIC Clouds, 2017.