Mark U. Wyse

phone: 425.614.8815 email: muwyse@gmail.com
web: homes.cs.washington.edu/~wysem

Education

University of Washington Seattle, WA June 2023 (Expected)
Paul G. Allen School of Computer Science & Engineering
PhD Computer Science & Engineering 3.79 GPA
Area: Computer Architecture, focusing on multicore memory systems and cache coherence
Advisor: Mark Oskin

University of Washington Seattle, WA Dec. 2015
M.S. Computer Science & Engineering 3.82 GPA
Area: Computer Architecture, focusing on approximate computing and hardware acceleration
Advisors: Luis Ceze and Mark Oskin

University of Washington Seattle, WA June 2014
B.S. Computer Engineering 3.89 GPA

Publications

Conference Papers:

Lost in Abstraction: Pitfalls of Analyzing GPUs at the Intermediate Language Level. Anthony Gutierrez, Bradford Beckmann, Alexandru Dutu, Joseph Gross, John Kalamatianos, Onur Kayiran, Michael Lebeane, Matthew Poremba, Brandon Potter, Sooraj Puthoor, **Mark Wyse**, Jieming Yin, Akshay Jain, Tim Rogers, Xianwei Zhang, Matthew Sinclair. HPCA 2018, February 2018. https://doi.org/10.1109/hpca.2018.00058

Compilation and Hardware Support for Approximate Acceleration. Thierry Moreau, Adrian Sampson, Andre Baixo, **Mark Wyse**, Ben Ransford, Jacob Nelson, Luis Ceze, Mark Oskin. TECHCON 2015.

SNNAP: Approximate Computing on Programmable SoCs via Neural Network Acceleration. Thierry Moreau, **Mark Wyse**, Jacob Nelson, Adrian Sampson, Hadi Esmaeilzadeh, Luis Ceze, Mark Oskin. HPCA 2015, February 2015. https://doi.org/10.1109/hpca.2015.7056066

Journal and Magazine Articles:

BlackParrot: An Agile Open-Source RISC-V Multicore for Accelerator SoCs. Daniel Petrisko, Farzam Gilani, **Mark Wyse**, Dai Cheol Jung, Scott Davidson, Paul Gao, Chun Zhao, Zahra Azad, Sadullah Canakci, Bandhav Veluri, Tavio Guarino, Ajay Joshi, Mark Oskin, Michael Bedford Taylor. IEEE MICRO, Volume 40, Issue 4. https://doi.org/10.1109/MM.2020.2996145

A Taxonomy of Approximate Computing Techniques. Thierry Moreau, Joshua San Miguel, **Mark Wyse**, James Bornholt, Armin Alaghi, Luis Ceze, Natalie Enright Jerger, Adrian Sampson. IEEE Embedded Systems Letters. October 2017. https://doi.org/10.1109/les.2017.2758679

Research Reports:

Understanding GPGPU Vector Register File Usage. **Mark Wyse**. Ph.D. Qualifying Evaluation Research Report. January 2018.

A Taxonomy of Approximate Computing Techniques. Thiery Moreau, Joshua San Miguel, **Mark Wyse**, James Bornholt, Luis Ceze, Natalie Enright Jerger, Adrian Sampson. UW CSE Technical Report UW-CSE-16-03-01. March 2016.

Modeling Approximate Computing Techniques. **Mark Wyse**. UW CSE MS Research Report. December 2015.

Workshop Papers:
REACT: A Framework for Rapid Exploration of Approximate Computing Techniques. **Mark Wyse**, Andre Baixo, Thierry Moreau, Bill Zorn, James Bornholt, Adrian Sampson, Luis Ceze, Mark Oskin. Workshop on Approximate Computing Across the Stack (WAX) 2015 (co-located with PLDI 2015), June 2015.

Research Experience

University of Washington Seattle, WA
Paul G. Allen School of Computer Science & Engineering
Research Assistant, BlackParrot RISC-V Multicore Processor Jan. 2018 – Present
PI: Michael Taylor, Advisor: Mark Oskin

- Lead architect and developer for BlackParrot's cache coherence system
- Designed and verified the BedRock cache coherence protocol in BlackParrot
- Implemented fixed-function and microcode programmable coherence engines for BedRock
- Research focuses on programmability within the cache coherence, memory, and un-core regions of multicore processors

Advanced Micro Devices (AMD) Research Bellevue, WA Jan. 2017 – Dec. 2017
Post-Grad Scholar, Hardware Programmability
Supervisor: Brad Beckmann

- Researched future GPU architectures and microarchitectures targeting General Purpose GPU (GPGPU) compute tasks, focusing on vector register file optimizations
- Contributed to development of open-source AMD GPGPU model for the gem5 simulator

Advanced Micro Devices (AMD) Research Bellevue, WA Feb. 2016 – Aug. 2016
Co-op Engineer, Hardware Programmability
Supervisor: Brad Beckmann

- Research internship focusing on hardware programmability and microarchitecture of GPU architectures targeting General Purpose GPU (GPGPU) compute tasks
- Microarchitecture research focusing on register allocation and management strategies and optimizations

Microsoft Research Redmond, WA June 2015 – Sept. 2015
Research Intern
Manager: Douglas Carmean

- Researched hardware acceleration of bioinformatics algorithms on FPGAs and data analysis for nanopore sequencers

University of Washington Seattle WA
Paul G. Allen School of Computer Science & Engineering
Research Assistant, SAMPA (Computer Architecture) group Jan. 2014 – Dec. 2015
Advisors: Mark Oskin and Luis Ceze

- Human Sensory Bandwidth and the ability of humans to understand information conveyed through haptic (vibrating) devices on the surface of the forearm
- Nanopore DNA sequencing data analysis techniques and preliminary investigation of hardware acceleration options
- Approximate computing and the implications of exposing error on computer architectures
- High level synthesis of hardware accelerators from C/C++ source, and the combination of approximation and acceleration

Teaching Experience

University of Washington Seattle WA
Paul G. Allen School of Computer Science & Engineering

Instructor, CSE 369 – Introduction to Digital Design Spring 2022 (upcoming)

- Course covers implementation, specification, and simulation of digital logic
- Topics include Boolean algebra, combinational and sequential digital circuits, use of FPGAs

Instructor, CSE 351 – The Hardware/Software Interface Winter 2018, 2021

- Enrollment: 112 (WI'18),105 (WI'21) students
- Managed Teaching Assistant staffs of 6 (WI'18) and 8 (WI'21)
- Course covers number and data representation, x86-64 assembly programming, procedures and executables, memory and caches, virtual memory, memory allocation, and an introduction to C programming

Teaching Assistant

CSEP 548 – Computer Architecture Autumn 2015

- Graduate class on computer architecture
- Topics include hardware/software interface, out-of-order execution, memory hierarchies, multiprocessing, GPU architecture, and warehouse-scale computing

CSE 471 – Computer Design & Organization Spring 2015

- Advanced undergraduate class on computer architecture
- Topics include branch prediction, out-of-order execution, memory hierarchies, and multiprocessing

CSE 467 – Advanced Digital Design Winter 2015

- Advanced undergraduate class on digital design
- Topics include logic synthesis and optimization, HDLs, and logic implementation for reconfigurable fabrics
- Class project was implementing a programmable GPU on a Programmable System-on-a-Chip (PSoC)

CSE 352 – Hardware Design & Implementation Autumn 2013

- Undergraduate class focused on digital logic design and implementation of algorithms for synthesis to FPGAs through Verilog RTL

CSE 351 – Hardware/Software Interface Winter 2013, Winter 2014

- Undergraduate class focused on basic computer systems architecture with an introduction to memory systems, assembly programming, and exceptional control flow

Internship/Work Experience

Amazon Seattle, WA June 2013 – Sept. 2013
SDE Intern, Amazon Web Services – Glacier

- Designed and implemented software to reduce customer archive upload failures
- Developed test plan for software project consisting of unit, integration, and network tests

Lockheed Martin Aeronautics Palmdale, CA June 2012 – Sept. 2012
College Tech Intern, Palmdale Site Flight Test

- Developed software integrating legacy C code with .NET using a mixed-mode C++/CLI wrapper library
- Supported real time flight test missions on multiple flight test programs

Lockheed Martin Aeronautics Fort Worth, TX June 2011 – Sept. 2011
College Tech Intern, F-35/JSF Flight Test Data Processing

- Developed data parsing programs for instrumentation configuration and testing in C#
- Revised and created processing procedure documentation for delivery to customers

Microsoft Redmond, WA June 2009 – Sept. 2009
High School Intern, Visual F# Language Team

- Developed sample code for inclusion in example packs distributed on MSDN
- Designed and implemented a Sudoku solver and UI to demonstrate interoperability of F# with other .NET entities

Microsoft Redmond, WA June 2008 – Sept. 2008
High School Intern, GFS Change & Release Management

- Developed reports for software change management to ensure high quality software release from Global Foundation Service (GFS) product teams

Technical Skills

Programming/Hardware Languages:

- Experienced: SystemVerilog/Verilog, C, Python, RISC-V assembly, *nix shell scripting, Make
- Familiar: C++, x86-64 assembly, TCL, JavaScript, C#, Java
- Past experience: HTML/CSS, Go, MATLAB

Frameworks, Tools, and Software:

- Experienced: Verilator, Linux, Git, Vim, MS Office
- Familiar: Synopsys VCS, gem5, Vivado Design Suite, Docker, QEMU, Visual Studio, D3.js
- Past experience: Intel PIN, Vivado HLS, Eclipse, Active-HDL, ModelSim Quartus II

Professional Affiliations & Service

Institute of Electrical and Electronics Engineers (IEEE), Student Member	2013 – present
Association for Computing Machinery (ACM), Student Member	2012 – present
UW CSE Undergrad Tutor	2016 – 2018
UW College of Engineering / CSE Department Volunteer	2012 – 2017
American Institute of Aeronautics and Astronautics (AIAA)	2009 – 2014
Lockheed Martin Leadership Association Super Science Saturday Volunteer	April 16, 2011

Awards & Honors

University of Washington, College of Engineering Dean's List	2012 – 2014
Cal Poly, President's Honors List	2011
Cal Poly, College of Engineering Dean's List	2010 – 2011
PACCAR Paul Pigott Scholarship Foundation Academic Scholarship	2009

References

Mark Oskin
oskin@cs.washington.edu
Associate Professor
University of Washington, Department of Computer Science & Engineering

Luis Ceze
luisceze@cs.washington.edu
Professor
University of Washington, Department of Computer Science & Engineering

Brad Beckmann
brad.beckmann@amd.com
Advanced Micro Devices (AMD) Research